Radhai Mahavidyalaya Aurangabad College of Computer science
& management science

Approved by Govt. of Maharashtra & Affilate to Dr. Babasaheb Ambedkar university Aurangabad.
Recognized Under Section 2(f) & 12 (B) of the U.G.C Act.
An ISO 9001-2015 Certified institution

DE Lab Manual

Student Name:……

RollNo :……

Branch:……..Section……

Year ……Semester…….

FACULTY INCHARGE

DIGITAL ELECTRONICS LAB

DO'S

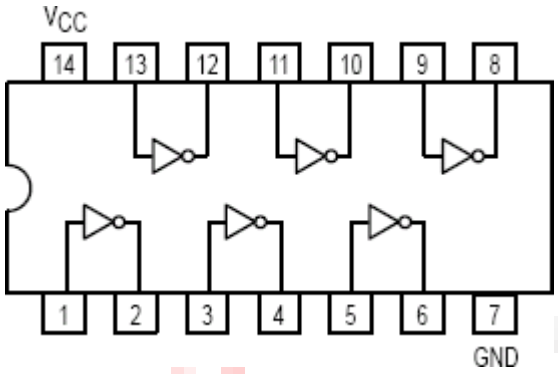
1. Be regular to the lab.
2. Follow proper Dress Code.
3. Maintain Silence.
4. Know the theory behind the experiment before coming to the lab.
5. Identify the different leads or terminals or pins of the IC before making connection.
6. Know the Biasing Voltage required for different families of IC's and connect the power supply voltage and ground terminals to the respective pins of the IC's.
7. Know the Current and Voltage rating of the IC's before using them in the experiment.
8. Avoid unnecessary talking while doingthe experiment.
9. Handle the IC Trainer Kit properly.
10. Mount the IC Properly on the IC Zif Socket.
11. Handle the microprocessor kitproperly.
12. While doing the Interfacing, connect proper voltages to the interfacing kit.
13. Keep the Table clean.
14. Take a signature of the In charge before taking the kit/components.
15. After the completion of the experiments switch off the power supply and return the apparatus.
16. Arrange the chairs/stools and equipment properly before leaving thelab.

DON' TS

1. Do not exceed the voltage Rating.
2. Do not inter change the IC's while doing the experiment.
3. Avoid loose connections and short circuits.
4. Do not throw the connecting wires to floor.
5. Do not come late to the lab.
6. Do not operate µp/IC trainer kits unnecessarily.
7. Do not panic if you don't get theoutput.

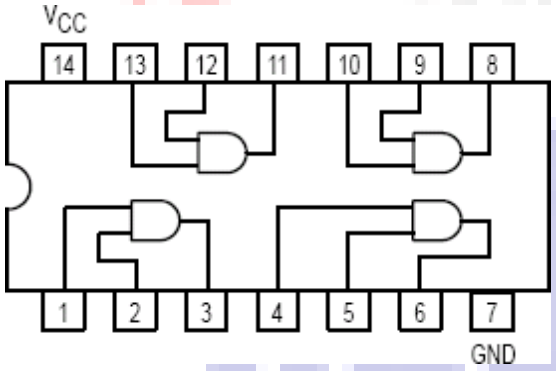
CONTENTS

Inverter Gate (NOT Gate) → 7404LS



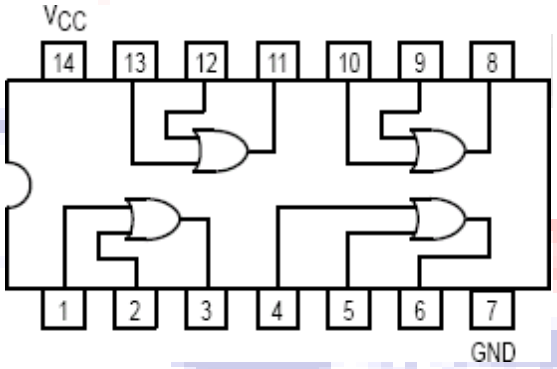
A	O/P	Y1 (V)	Y2 (V)	Y3 (V)	Y4 (V)	Y5 (V)	Y6 (v)
0	1						
1	0						

2-Input AND Gate → 7408LS



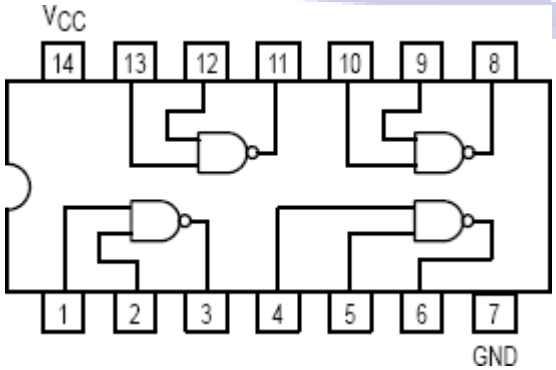
A	B	O/P	Y1 (V)	Y2 (V)	Y3 (V)	Y4 (V)
0	0	0				
0	1	0				
1	0	0				
1	1	1				

2-Input OR Gate → 7432LS



A	B	O/P	Y1 (V)	Y2 (V)	Y3 (V)	Y4 (V)
0	0	0				
0	1	0				
1	0	0				
1	1	1				

2-Input NAND Gate → 7400LS



A	B	O/P	Y1 (V)	Y2 (V)	Y3 (V)	Y4 (V)
0	0	1				
0	1	0				
1	0	0				
1	1	0				

Experiment No: **Date:__/__/____**

VERIFICATION OF GATES

Aim: - To study and verify the truth table of logic gates

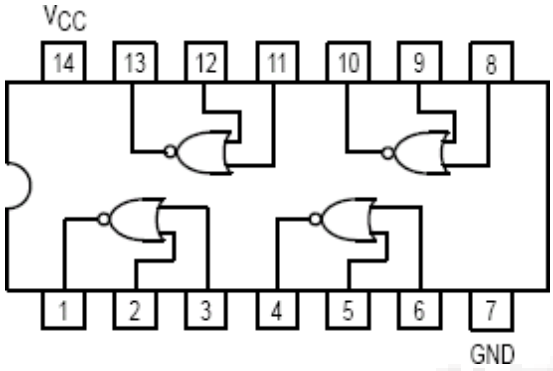
Apparatus Required: -

All the basic gates mention in the fig.

Procedure: -

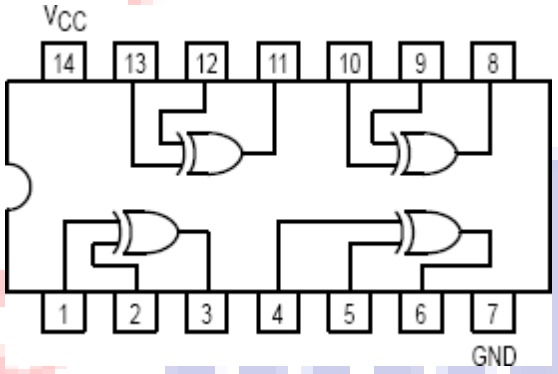
1. **Place the IC on IC Trainer Kit.**
2. **Connect V_{CC} and ground to respective pins of IC Trainer Kit.**
3. **Connect the inputs to the input swit ches provided in the IC Trainer Kit.**
4. **Connect the outputs to the switches of O/P LEDs,**
5. **Apply various combinations of inputs according to the truth table and observe condition of LEDs.**
6. **Disconnect output from the LEDs and note down the corresponding multimeter voltage readings for various combinations of inputs.**

2-Input NOR Gate → 7402LS



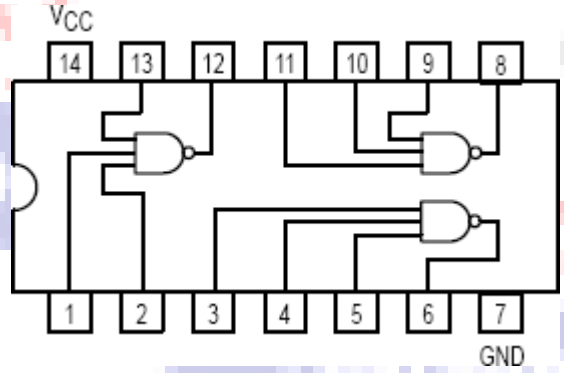
A	B	O/P	Y1 (V)	Y2 (V)	Y3 (V)	Y4 (V)
0	0	1				
0	1	0				
1	0	0				
1	1	0				

2- Input EX-OR Gate → 7486LS



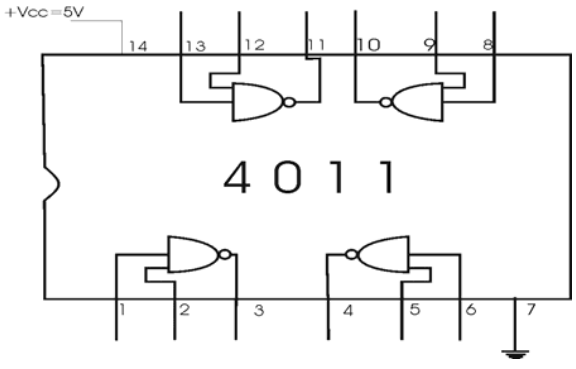
A	B	O/P	Y1 (V)	Y2 (V)	Y3 (V)	Y4 (V)
0	0	0				
0	1	1				
1	0	1				
1	1	0				

3- Input NAND Gate → 7410LS



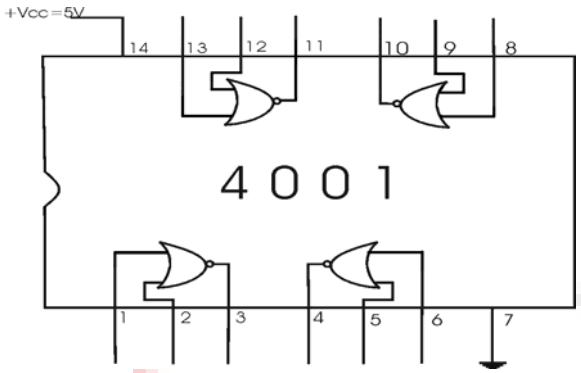
A	B	C	O/P	Y1 (V)	Y2 (V)	Y3 (V)
0	0	0	1			
0	0	1	1			
0	1	0	1			
0	1	1	1			
1	0	0	1			
1	0	1	1			
1	1	0	1			
1	1	1	0			

2-Input NAND Gate → CD4011



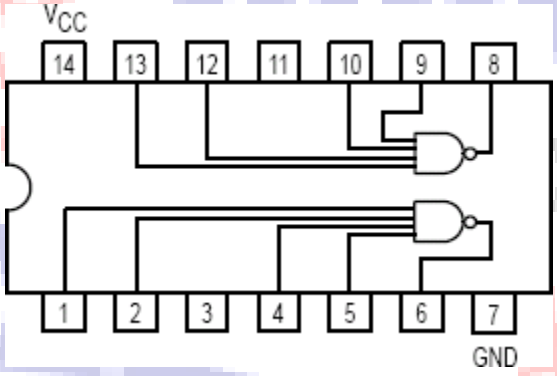
A	B	O/P	Y1 (V)	Y2 (V)	Y3 (V)	Y4 (V)
0	0	1				
0	1	1				
1	0	1				
1	1	0				

2-Input NOR Gate → CD4001



A	B	O/P	Y1 (V)	Y2 (V)	Y3 (V)	Y4 (V)
0	0	1				
0	1	0				
1	0	0				
1	1	0				

4-Input NAND Gate → 7420LS



A	B	C	D	O/P	Y1 (V)	Y2 (V)	Y3 (V)
0	0	0	0	1			
0	0	0	1	1			
0	0	1	0	1			
0	0	1	1	1			
0	1	0	0	1			
0	1	0	1	1			
0	1	1	0	1			
0	1	1	1	1			
1	0	0	0	1			
1	0	0	1	1			
1	0	1	0	1			
1	0	1	1	1			
1	1	0	0	1			
1	1	0	1	1			
1	1	1	0	1			
1	1	1	1	0			

Conclusion:-

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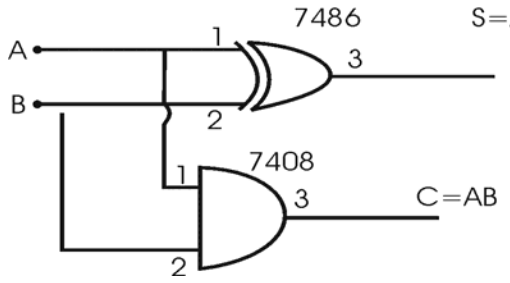
Signature of the staff

Half Adder using basic gates:-

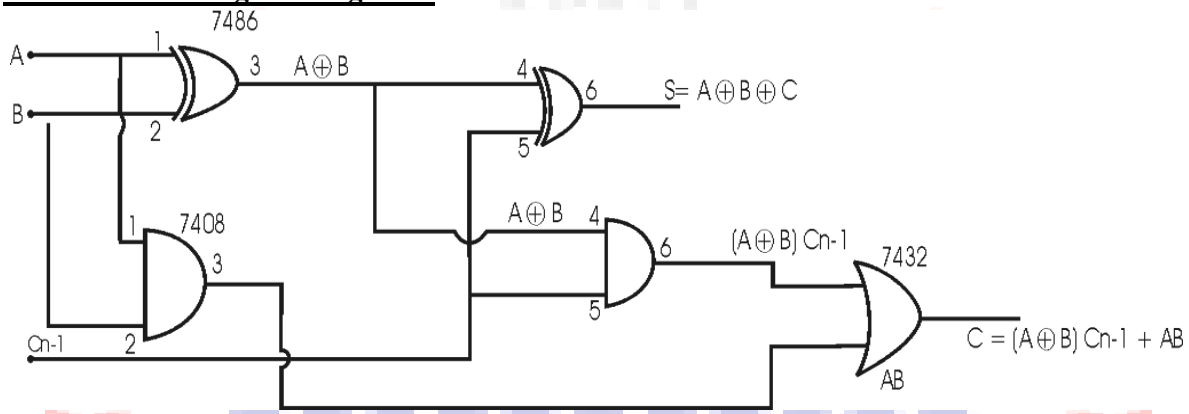


$S = \bar{A}B + A\bar{B}$

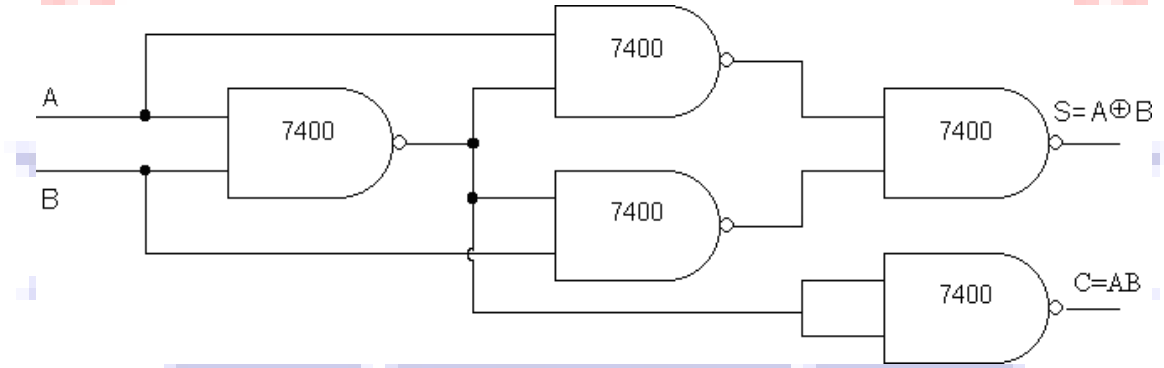
$S = A \oplus B$

$C = AB$

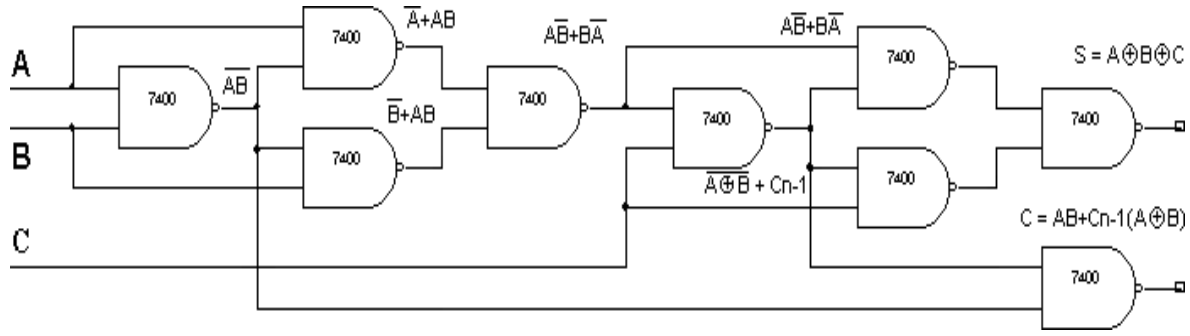
Full Adder using basic gates:-



Half Adder using NAND gates only:-



Full Adder using NAND gates only:-



Experiment No: **Date:__/__/____**

HALF/FULL ADDER & HALF/FULL SUBTRACTOR

Aim: - To realize half/full adder and half/full subtractor.

i. **Using X-OR and basic gates**

ii. **Using only nand gates.**

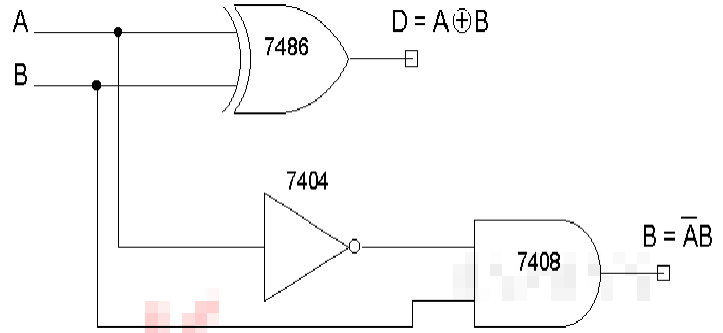
Apparatus Required: -

IC 7486, IC 7432, IC 74 08, IC 7400, etc.

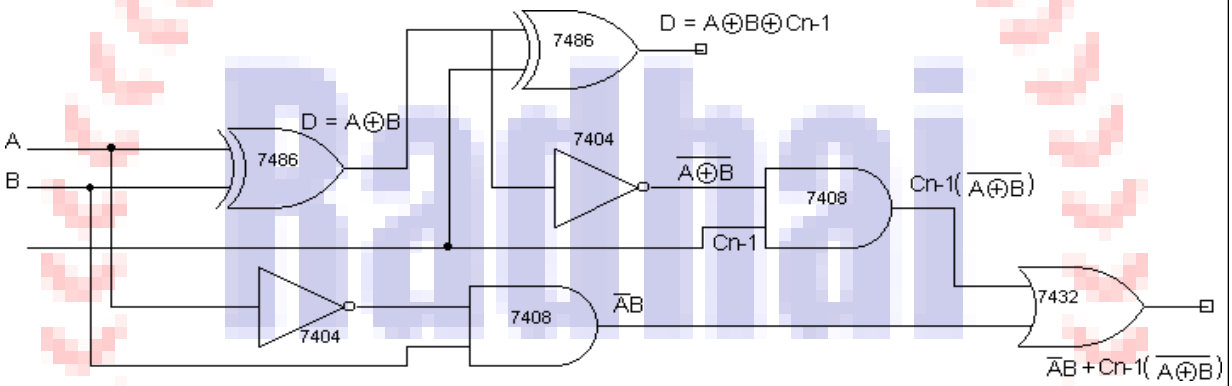
Procedure: -

1. **Verify the gates.**
2. **Make the connections as per the circuit diagram.**
3. **Switch on V_{CC} and apply various combinations of input according to the truth table.**
4. **Note down the output readings fo r half/full adder and half/full subtractor sum/difference and the carry/borrow bit for different combinations of inputs.**

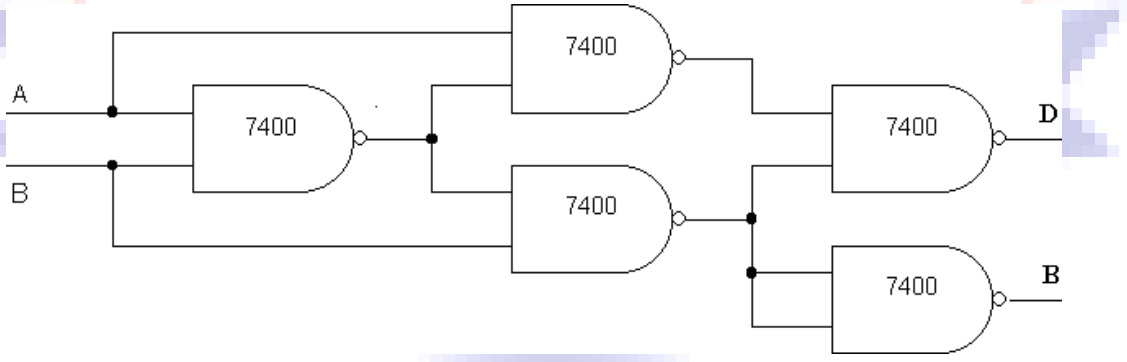
Using X – OR and Basic Gates (a)Half Subtractor



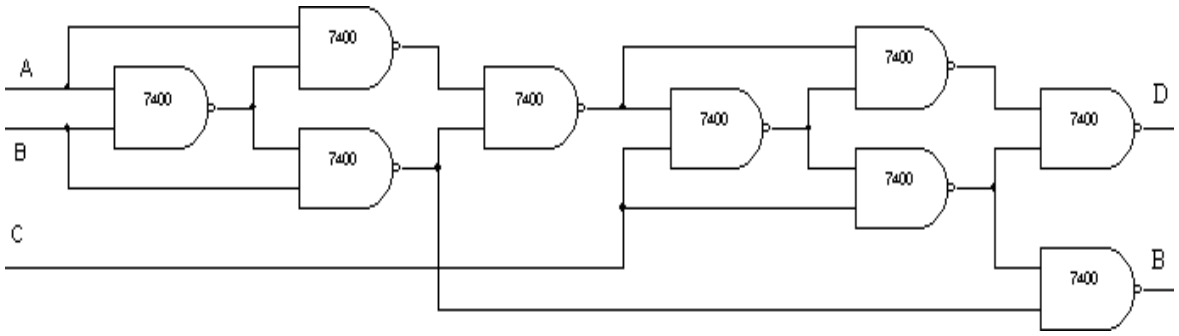
Full Subtractor



(ii) Using only NAND gates (a) Half subtractor



(b) Full Subtractor



Half Adder					
A	B	S	C	S(V)	C(V)
	0	0	0		
0	1	1	0		
1	0	1	0		
1	1	0	1		

Half Subtractor					
A	B	D	B	D(V)	B(V)
0	0	0	0		
0	1	1	1		
1	0	1	0		
1	1	0	0		

Full Adder						
A	B	Cn-1	S	C	S(V)	C(V)
0	0	0	0	0		
0	0	1	1	0		
0	1	0	1	0		
0	1	1	0	1		
1	0	0	1	0		
1	0	1	0	1		
1	1	0	0	1		
1	1	1	1	1		

Full Subtractor						
A	B	Cn-1	D	B	D(v)	B(v)
0	0	0	0	0		
0	0	1	1	1		
0	1	0	1	1		
0	1	1	0	1		
1	0	0	1	0		
1	0	1	0	0		
1	1	0	0	0		
1	1	1	1	1		

Conclusion: -

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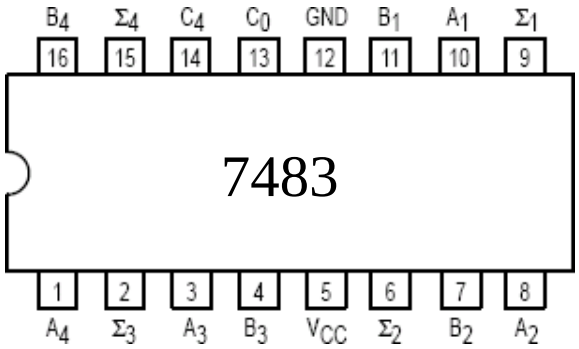
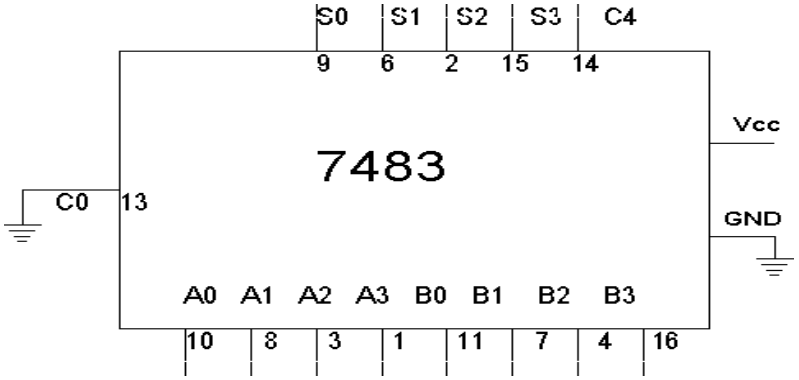
Signature of the staff in charge

Pin Detail: -



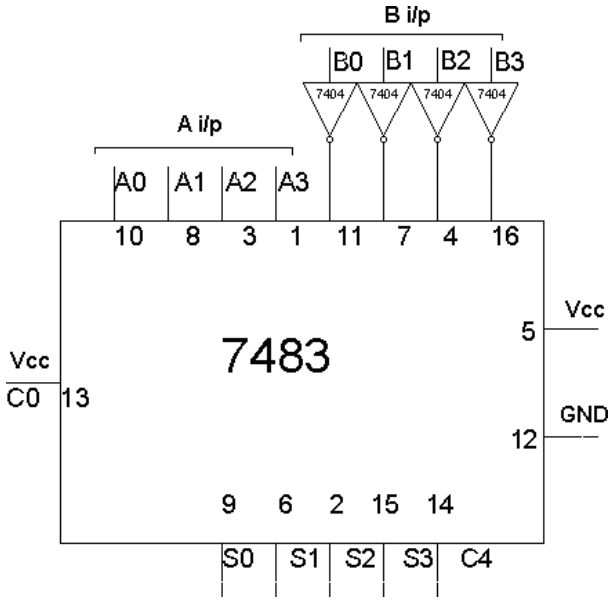
Adder : -



Truth Table: -

A3	A2	A1	A0	B3	B2	B1	B0	C4 (V)	S3(V)	S2(V)	S1(V)	S0(V)
0	0	0	1	0	0	1	0	0	0	0	1	1
0	1	0	1	1	0	1	1	1	1	0	0	0
1	0	1	0	1	0	1	0	1	0	1	0	0
1	1	1	1	1	1	1	1	1	1	1	1	0
0	1	1	1	0	0	1	1	0	1	0	1	0

Subtractor:-



Experiment No: **Date:__/__/____**

PARALLEL ADDER AND SUBTRACTOR USING 7483

Aim: - **To realize IC7483 as parallel adder / Subtractor.**

Apparatus Required: -

IC 7483, IC 7404, etc.

Procedure: -

1. **Apply the inputs to A0 to A3 and B0 to B3.**
2. **Connect C0 to the Ground.**
3. **Check the output sum on the S0 to S3 and also C4.**
4. **For subtraction connect C0 to Vcc, Apply the B input through NOT gate, which gives the complement of B.**
5. **The truth table of adder and Subtractor are noted down.**

Truth Table for Subtractor

A3	A2	A1	A0	B3	B2	B1	B0	C4(V)	S3(V)	S2(V)	S1(V)	S0(V)
0	0	1	0	0	0	0	1	1	0	0	0	1
0	1	0	1	0	0	1	1	1	0	0	1	0
0	0	1	1	0	1	0	1	0	1	1	1	0

1	**0**	**1**	**0**	**0**	**1**	**1**	**0**	**1**	**0**	**1**	**0**	**0**
1	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**0**	**1**	**0**	**0**	**1**

Conclusion: -

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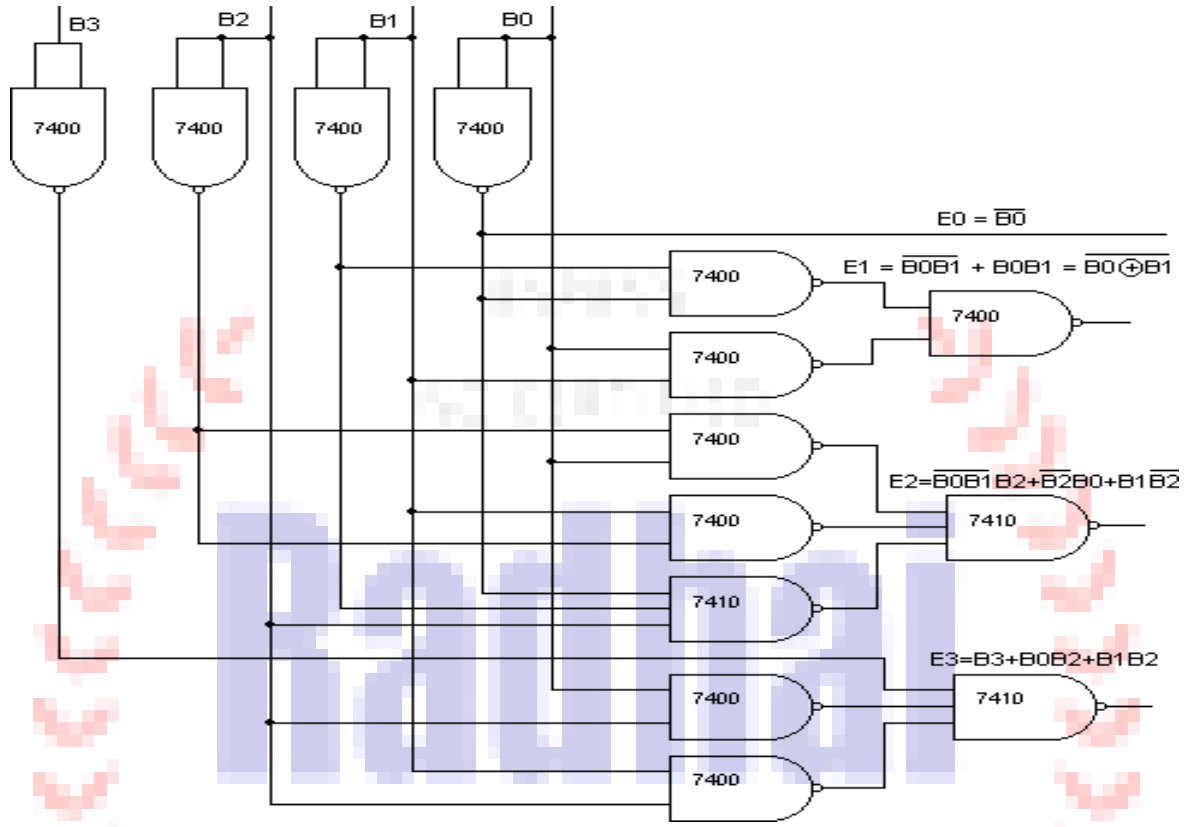
Signature of the staff

BCD To Excess-3



Truth Table For Code Conversion: -

Inputs				Outputs			
B3	B2	B1	B0	E3 (v)	E2 (v)	E1 (v)	E0 (v)
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

Experiment No: **Date:__/__/____**

BCD to Excess 3 AND Excess 3 to BCD

Aim: - **To verify BCD to excess –3 code conv ersion using NAND gates. To study and verify the truth table of excess-3 to BCD code converter**

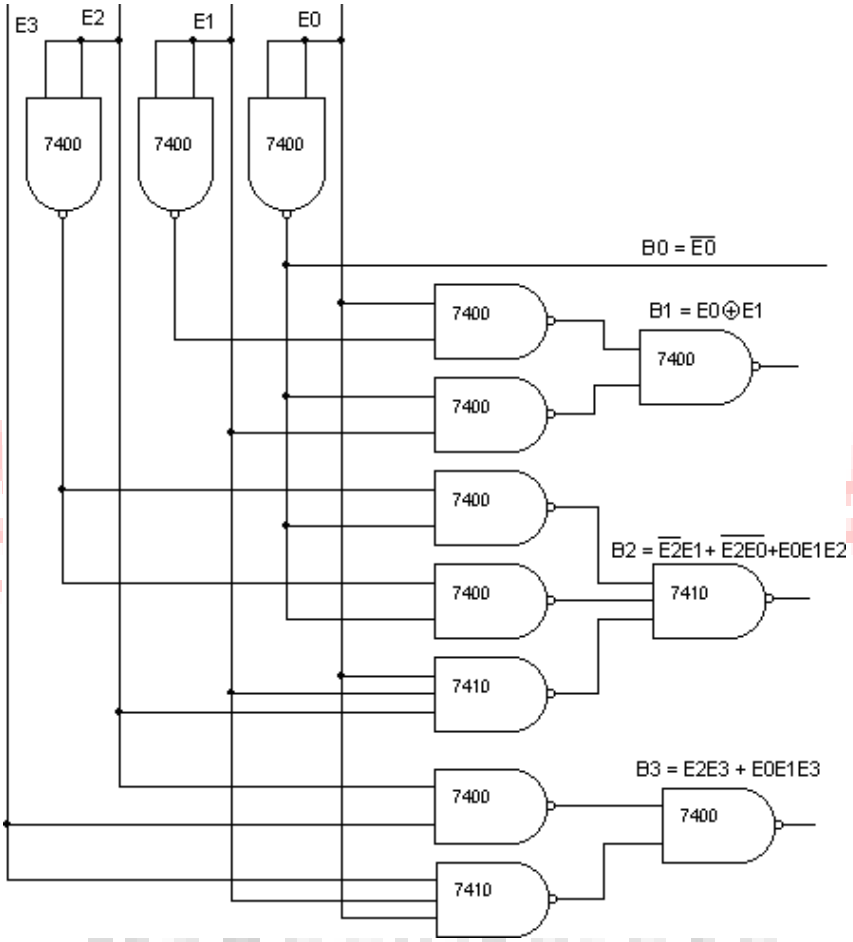
Apparatus Required: -

IC 7400, IC 7404, etc.

Procedure: - (BCD Excess 3 and Vice Versa)

1. **Make the connections as shown in the fig.**
2. **Pin [14] of all IC'S are connected to +5V and pin [7] to the ground.**
3. **The inputs are applied at E3, E2, E1, and E0 and the corresponding outputs at B3, B2, B1, and B0 ar e taken for excess – 3 to BCD.**
4. **B3, B2, B1, and B0 are the inputs an d the corresponding outputs are E3, E2, E1 and E0 for BCD to excess – 3.**
5. **Repeat the same procedure for other combinations of inputs.**
6. **Truth table is written.**

Excess-3 To BCD :-



Truth Table For Code Conversion: -

Inputs				Outputs			
E3	**E2**	**E1**	**E0**	**B3 (v)**	**B2 (v)**	**B1 (v)**	**B0(v)**
0	**0**	**1**	**1**	**0**	**0**	**0**	**0**
0	**1**	**0**	**0**	**0**	**0**	**0**	**1**
0	**1**	**0**	**1**	**0**	**0**	**1**	**0**
0	**1**	**1**	**0**	**0**	**0**	**1**	**1**
0	**1**	**1**	**1**	**0**	**1**	**0**	**0**
1	**0**	**0**	**0**	**0**	**1**	**0**	**1**
1	**0**	**0**	**1**	**0**	**1**	**1**	**0**
1	**0**	**1**	**0**	**0**	**1**	**1**	**1**
1	**0**	**1**	**1**	**1**	**0**	**0**	**0**
1	**1**	**0**	**0**	**1**	**0**	**0**	**1**

Exercise: -

1. **Obtain the expression for E3, E2, E1 and E0**

2. **Obtain the expression for B3, B2, B1 and B0**

Conclusion: -

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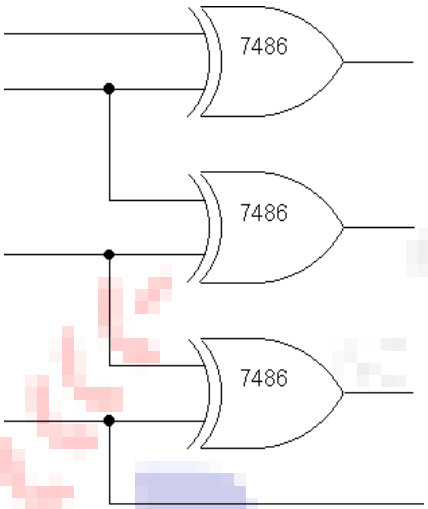
Signature of the staff-in charge

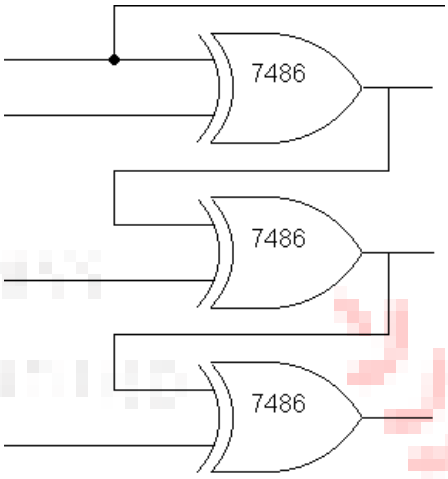
Circuit Diagram: -

Binary To Gray



Using EX-OR gates

Gray To Binary



Using EX-OR gates

Truth Table For Both: -

Inputs				Outputs			
B3	**B2**	**B1**	**B0**	**G3 (V)**	**G2 (V)**	**G1 (V)**	**G0 (V)**
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

Experiment No: **Date:__/__/____**

BINARY TO GRAY AND GRAY TO BINARY CONVERSION

Aim: - To convert given binary numbers to gray codes.

Apparatus Required: -

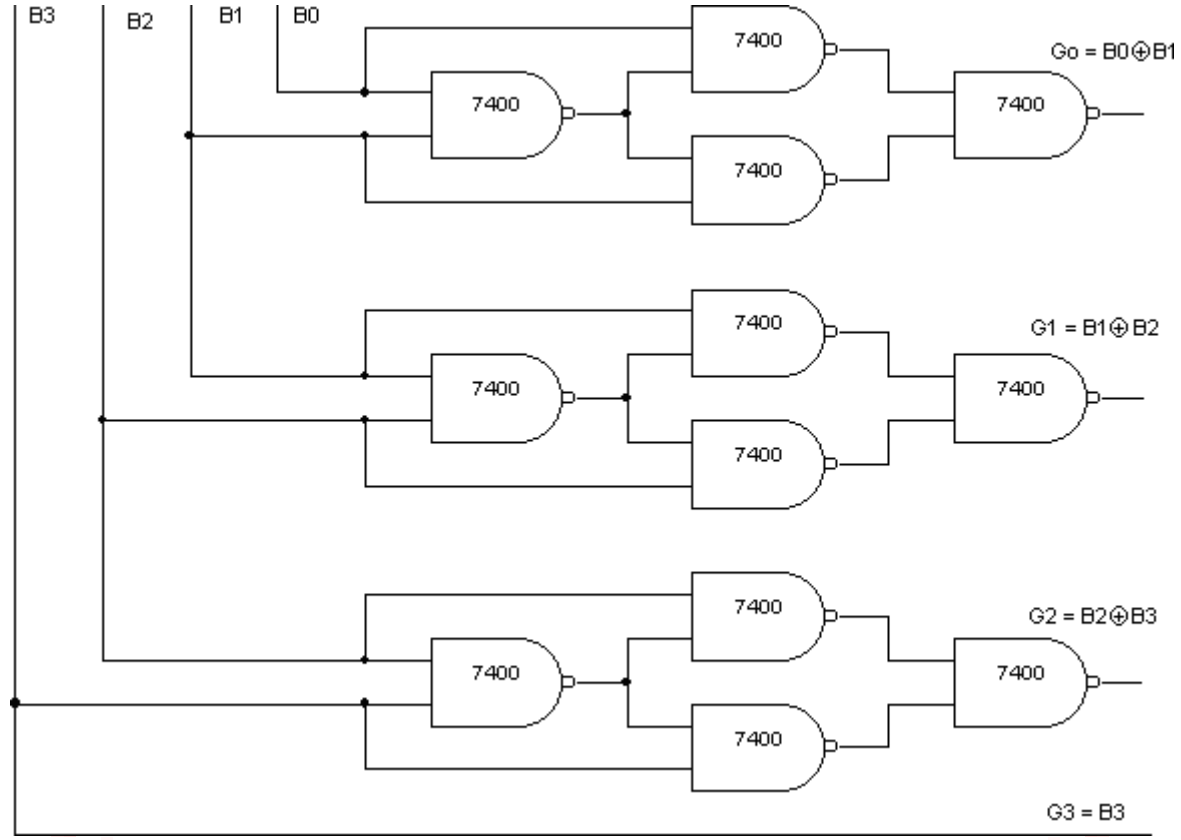
IC 7486, etc

Procedure: -

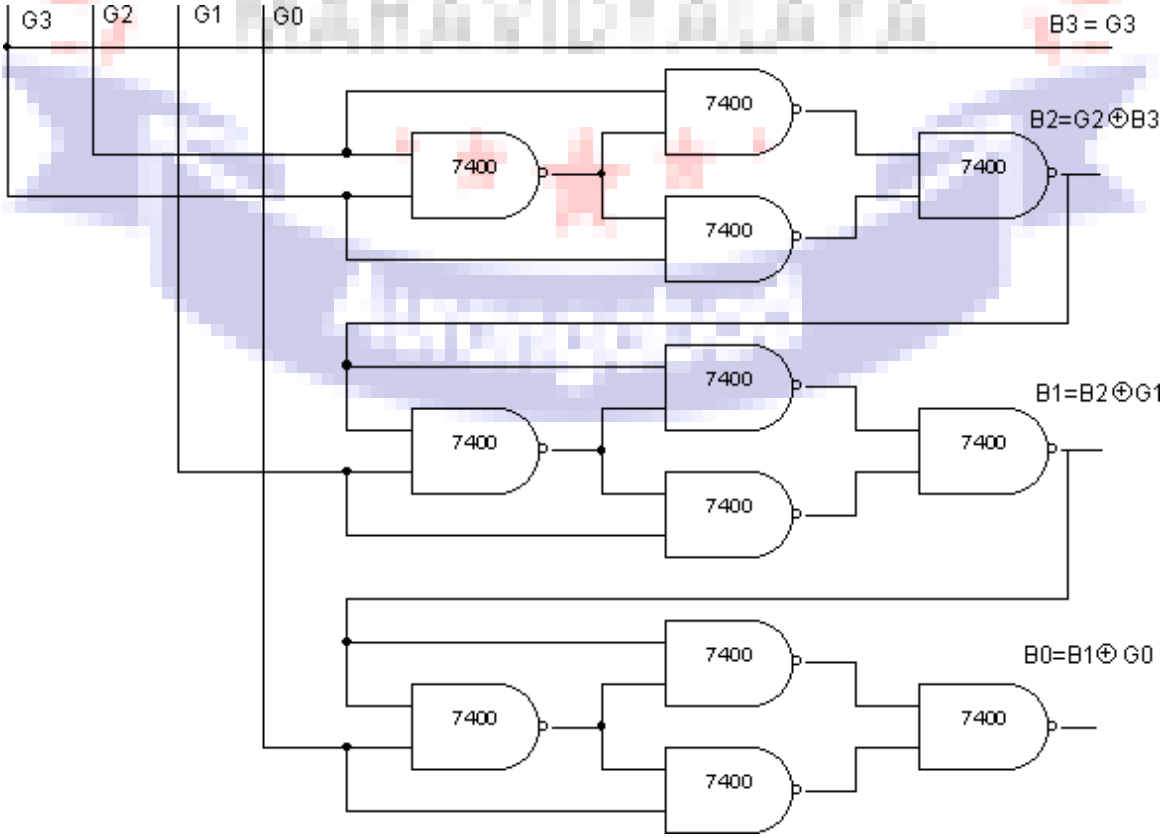
1. **The circuit connections are made as shown in fig.**
2. **Pin (14) is connected to +Vcc and Pin (7) to ground.**
3. **In the case of binary to gray conver sion, the inputs B0, B1, B2 and B3 are given at respective pins and outputs G0, G1, G2, G3 are taken for all the 16 combinations of the input.**
4. **In the case of gray to binary conver sion, the inputs G0, G1, G2 and G3 are given at respective pins and outputs B0, B1, B2, and B3 are taken for all the 16 combinations of inputs.**
5. **The values of the outputs are tabulated.**

Using Nand Gates Only: -

Binary To Gray



Gray To Binary



Truth Table For Both: -

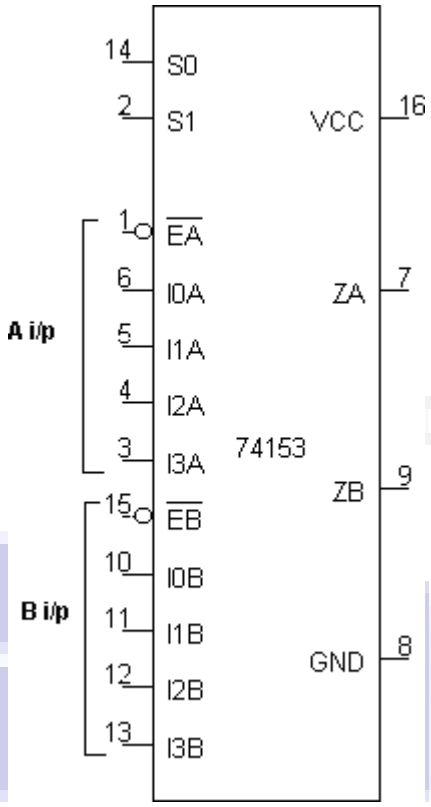
Inputs				Outputs			
B3	B2	B1	B0	G3 (V)	G2 (V)	G1 (V)	G0 (V)
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	0	0
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	1
1	0	1	1	1	1	1	0
1	1	0	0	1	0	1	0
1	1	0	1	1	0	1	1
1	1	1	0	1	0	0	1
1	1	1	1	1	0	0	0

Conclusion: -

.....

Signature of the staff in charge

Pin Details: -



Truth Table: -

CHANNEL – A								CHANNEL – B							
INPUTS					SELECT LINES		O/P	INPUTS					SELECT LINES		O/P
Ēa	Ioa	I1a	I2a	I3a	S1	S2	Za(v)	Ēa	Iob	I1b	I2b	I3b	S1	S2	Za(v)
1	X	X	X	X	X	X	0	1	X	X	X	X	X	X	0
0	0	X	X	X	0	0	0	0	0	X	X	X	0	0	0
0	1	X	X	X	0	0	1	0	1	X	X	X	0	0	1
0	X	0	X	X	0	1	0	0	X	0	X	X	0	1	0
0	X	1	X	X	0	1	1	0	X	1	X	X	0	1	1
0	X	X	0	X	1	0	0	0	X	X	0	X	1	0	0
0	X	X	1	X	1	0	1	0	X	X	1	X	1	0	1
0	X	X	X	0	1	1	0	0	X	X	X	0	1	1	0
0	X	X	X	1	1	1	1	0	X	X	X	1	1	1	1

Experiment No: **Date: __/_/____**

MUX/DEMUX USING 74153 & 74139

Aim: - To verify the truth table of multiplexer using 74153 & to verify a demultiplexer using 74139. To study the arithmetic circuits half-adder half Subtractor, full adder and full Subtractor using multiplexer.

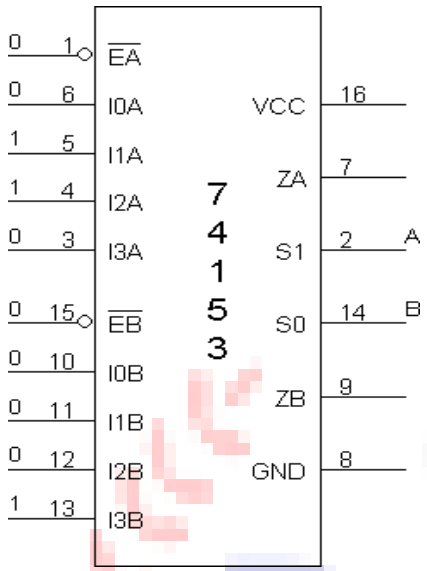
Apparatus Required: -

IC 74153, IC 74139, IC 7404, etc.

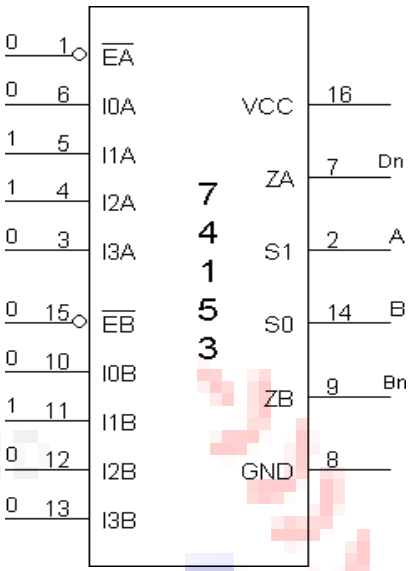
Procedure: - (IC 74153)

1. **The Pin [16] is connected to + Vcc.**
2. **Pin [8] is connected to ground.**
3. **The inputs are applied either to 'A' input or 'B' input.**
4. **If MUX 'A' has to be initialized, Ea is made low and if MUX 'B' has to be initialized, E_b is made low.**
5. **Based on the selection lines one of the inputs will be selected at the output and thus the truth table is verified.**
6. **In case of half adder using MUX, sum and carry is obtained by applying a constant inputs at I_{0a}, I_{1a}, I_{2a}, I_{3a} and I_{0b}, I_{1b}, I_{2b} and I_{3b} and the corresponding values of select lines are changed as per table and the output is taken at Z0a as sum and Z0b as carry.**
7. **In this case, the channels A and B are kept at constant inputs according to the table and the inputs A and B are varied. Making Ea and Eb zero and the output is taken at Za, and Zb.**
8. **In full adder using MUX, the input is applied at Cn-1, An and Bn. According to the table corresponding outputs are taken at Cn and Dn.**

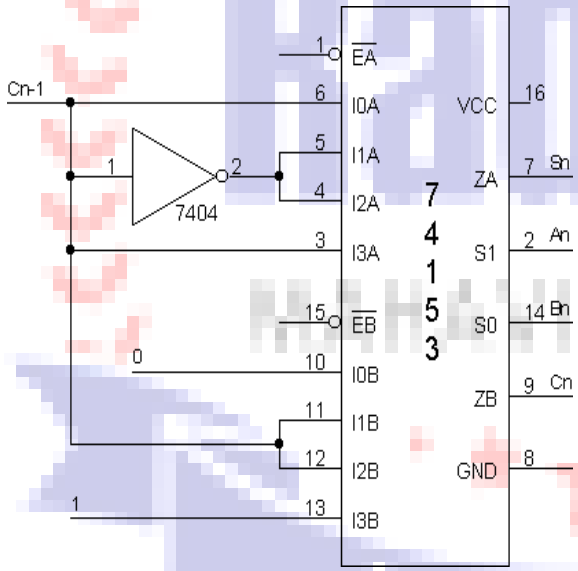
Half Adder Using 74153 –



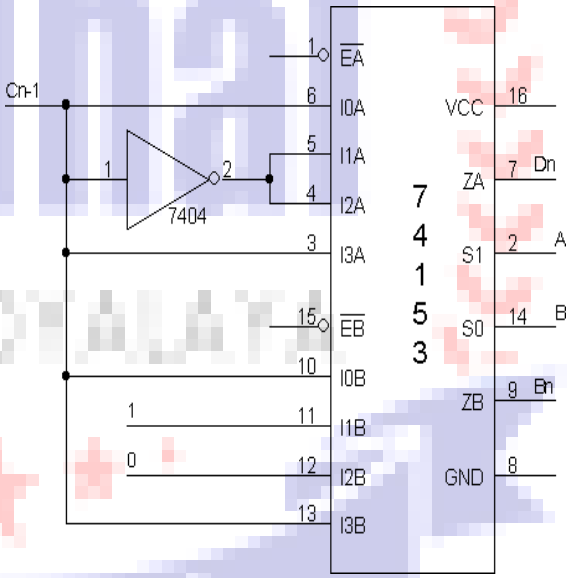
Half Subtractor: -



Full Adder Using 74153: -



Full Subtractor Using 74153: -



Truth Tables: - Same for both Subtractor and adder

Half adder/subtractor			
A	**B**	**Sn/Dn (V)**	**Cn/Bn (V)**
0	**0**		
0	**1**		
1	**0**		
1	**1**		

Full Adder/subtractro				
An	**Bn**	**Cn-1**	**Sn/Dn (V)**	**Cn/Bn (V)**
0	**0**	**0**		
0	**0**	**1**		
0	**1**	**0**		
0	**1**	**1**		
1	**0**	**0**		
1	**0**	**1**		
1	**1**	**0**		
1	**1**	**1**		

Pin Details: -

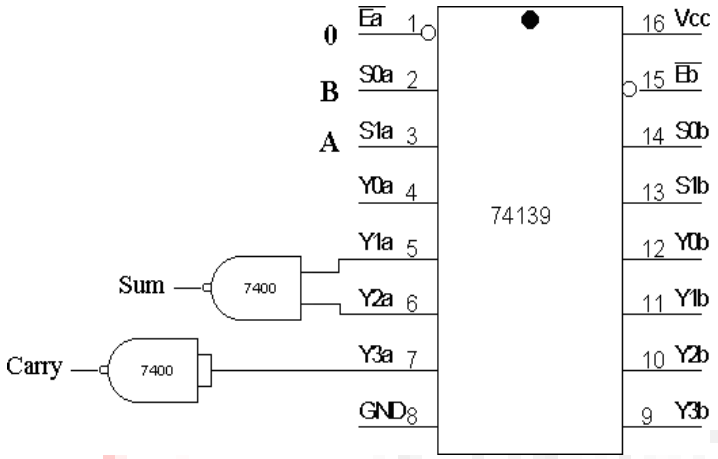
Truth Table For Demux: -

CHANNEL – A							CHANNEL – B						
Inputs			Outputs				Inputs			Outputs			
$\bar{E}a$	S1a	S0a	Y0a	Y1a	Y2a	Y3a	$\bar{E}b$	S1b	S0b	Y0b	Y1b	Y2b	Y3b
1	X	X	1	1	1	1	1	X	X	1	1	1	1
0	0	0	0	1	1	1	0	0	0	0	1	1	1
0	0	1	1	0	1	1	0	0	1	1	0	1	1
0	1	0	1	1	0	1	0	1	0	1	1	0	1
0	1	1	1	1	1	0	0	1	1	1	1	1	0

Procedure: - (IC 74139)

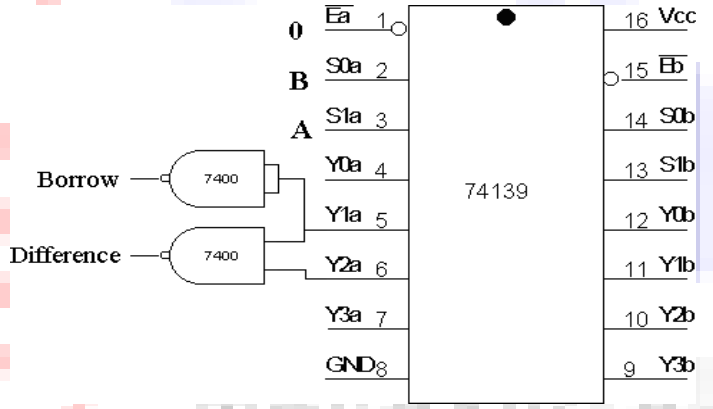
1. **The inputs are applied to either ‘a’ input or ‘b’ input**
2. **The demux is activated by making Ea low and Eb low.**
3. **The truth table is verified.**

Half adder



Half Adder			
A	B	Sn (V)	Cn (V)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

Half subtractor:-

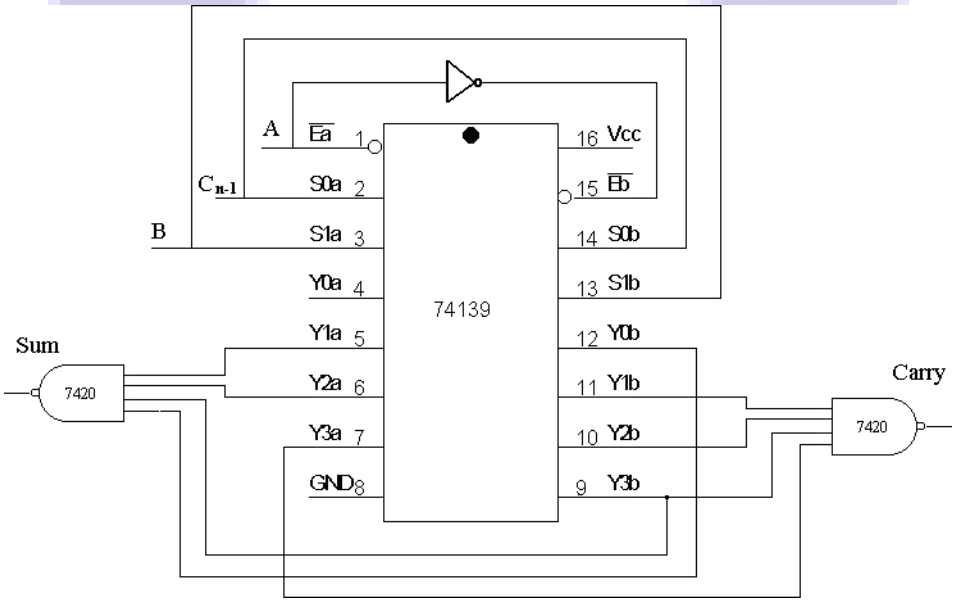


Half Subtractor			
A	B	Dn (V)	Bn (V)
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

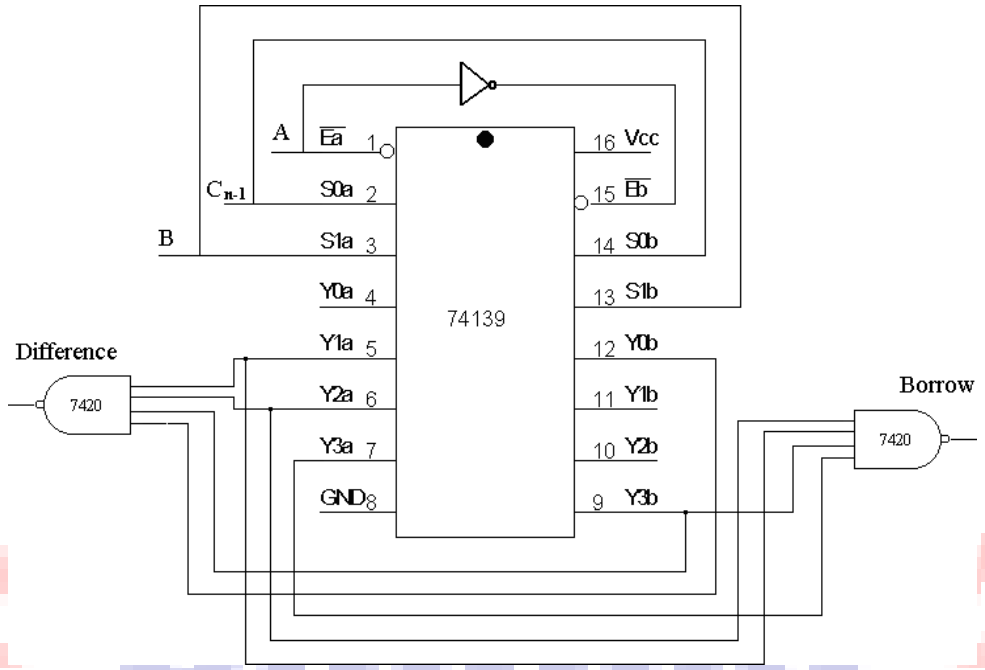
Exercise:-

- **Repeat the experiment to verify Channel B.**

Full Adder using IC 74139:-



Full subtractor using IC 74139:-



Truth Tables:-

Full Adder				
An	Bn	Cn-1	Sn (V)	Cn (V)
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Full Subtractor				
An	Bn	Cn-1	Dn (V)	Bn (V)
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Conclusion:-

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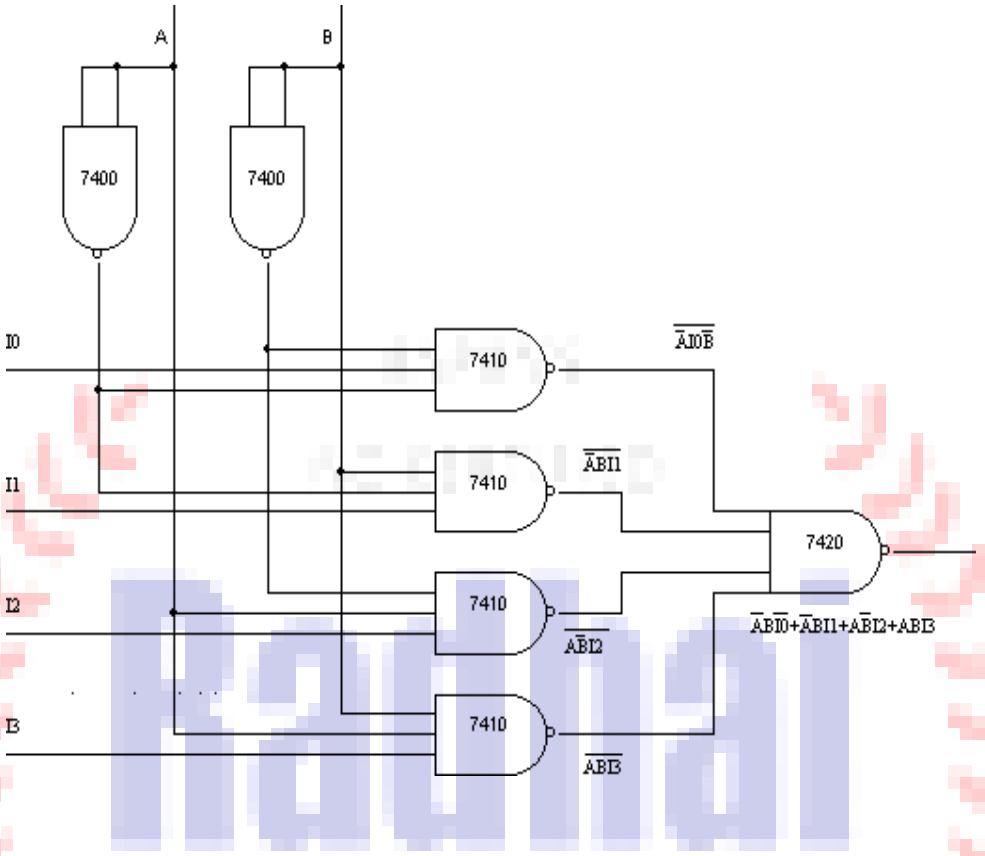
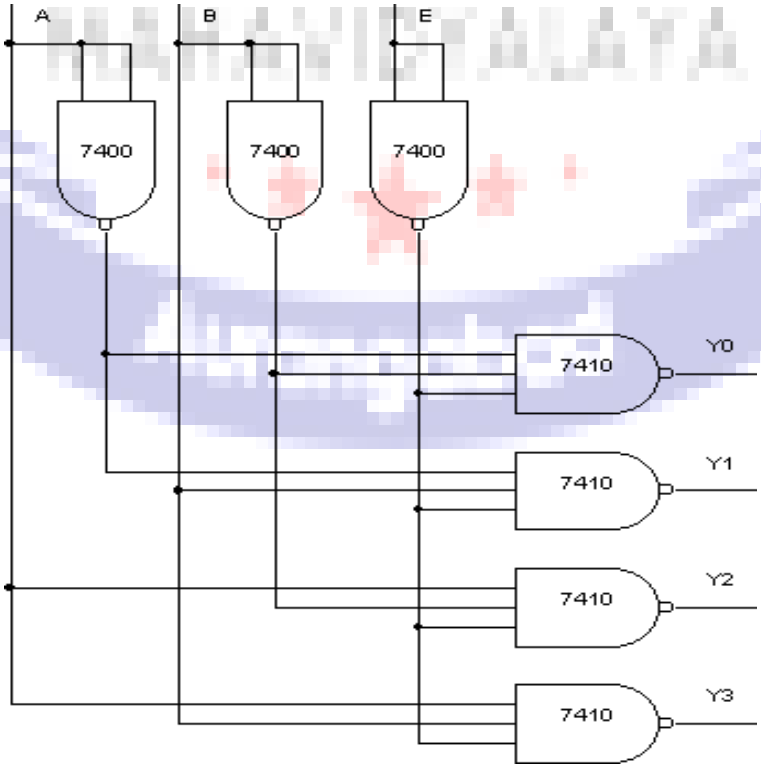
Signature of the staff in charge

MUX USING NAND GATES ONLY: -



DEMUX USING NAND GATES ONLY: -



Experiment No: **DATE: ___/_/_____**

MUX AND DEMUX USING NAND GATES

AIM: - To verify the truth table of MUX and DEMUX using NAND.

APPARATUS REQUIRED: -

IC 7400, IC 7410, IC 7420, etc.

PROCEDURE: -

1. **Connections are made as shown in the Circuit diagram.**
2. **Change the values of the inputs as per the truth table and note down the outputs readings using multimeter.**

TRUTH TABLES: -

INPUT						OUPUT
A	B	I0	I1	I2	I3	Y (V)
0	0	0	X	X	X	0
0	0	1	X	X	X	1
0	1	X	0	X	X	0
0	1	X	1	X	X	1
1	0	X	X	0	X	0
1	0	X	X	1	X	1
1	1	X	X	X	0	0
1	1	X	X	X	1	1

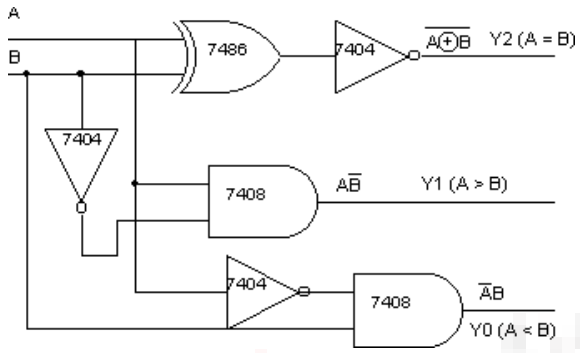
INPUT			OUPUT			
$\bar{E}$	A	B	Y0 (V)	Y1 (V)	Y2 ()	Y3 (V)
1	X	X	1	1	1	1
0	0	0	0	1	1	1
0	0	1	1	0	1	1
0	1	0	1	1	0	1
0	1	1	1	1	1	0

Conclusion:-

……

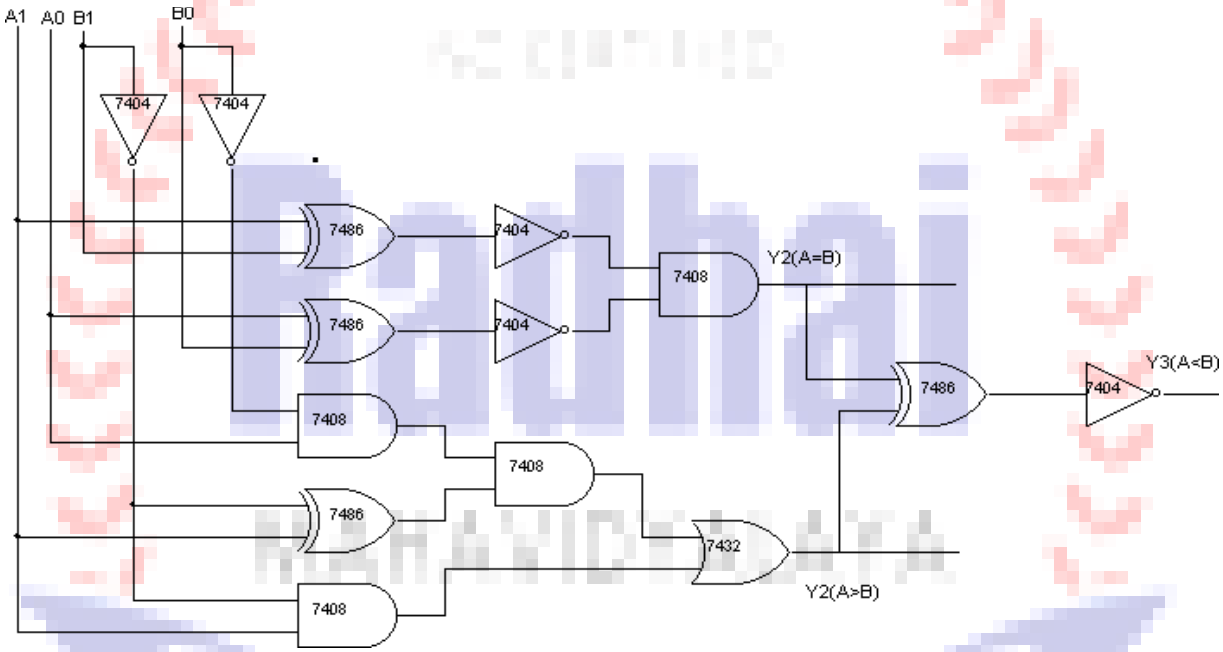
Signature of the staff in charge

One Bit Comparator: -



A	B	Y1 (A>B)	Y2 (A = B)	Y3 (A < B)
0	0	0	1	0
0	1	0	0	1
1	0	1	0	0
1	1	0	1	0

Two Bit Comparator: -



Two-Bit Comparator: -

A1	A0	B1	B0	Y1 (A > B)	Y2 (A = B)	Y3 (A < B)
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	0	1	0

Experiment No: **Date:__/__/____**

COMPARATORS

Aim: - To verify the truth t able of one bit and two bit comparators using logic gates.

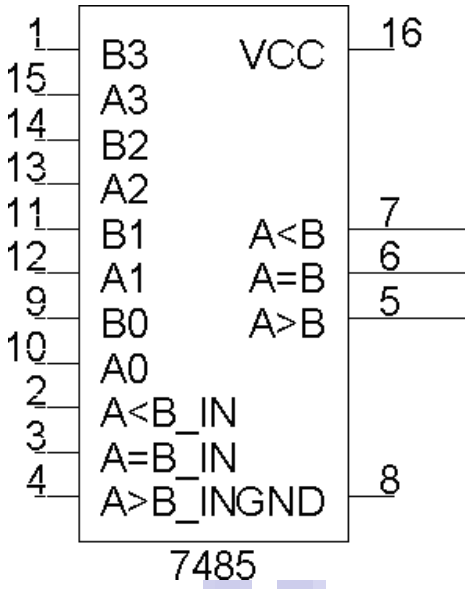
Apparatus Required: -

IC 7486, IC 7404, IC 7408, et c.

Procedure: -

1. **Verify the gates.**
2. **Make the connections as per the circuit diagram.**
3. **Switch on Vcc.**
4. **Applying i/p and Check for the outputs.**
5. **The voltameter readings of outputs are taken and tabulated in tabular column.**
6. **The o/p are verified.**

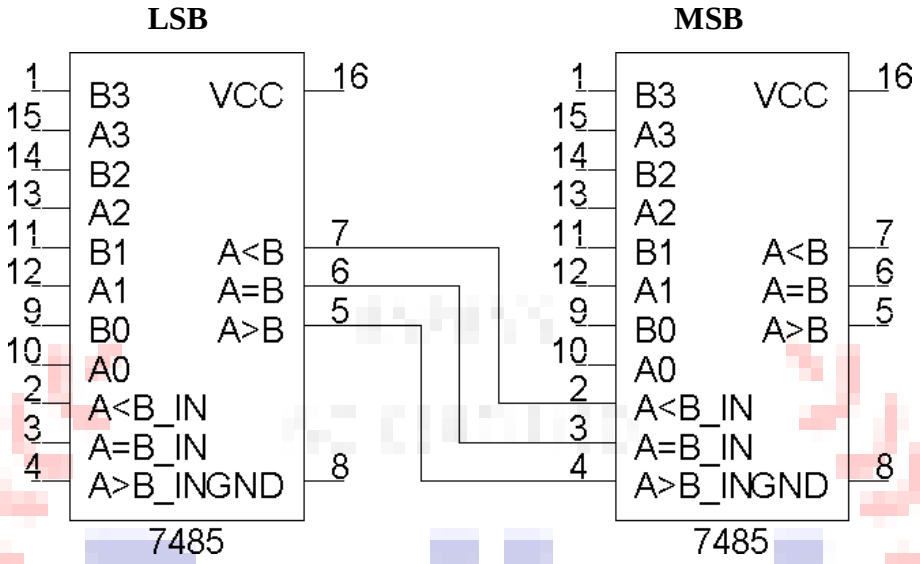
4-bit Comparator



Tabular Coloumn For 8-Bit Comparator: -

A_3 B_3	A_2 B_2	A_1 B_1	A_0 B_0	A>B	A=B	A<B	A>B	A=B	A<B
$A_3>B_3$	X	X	X	X	X	X			
$A_3<B_3$	X	X	X	X	X	X			
$A_3=B_3$	$A_2>B_2$	X	X	X	X	X			
$A_3=B_3$	$A_2<B_2$	X	X	X	X	X			
$A_3=B_3$	$A_2=B_2$	$A_1>B_1$	X	X	X	X			
$A_3=B_3$	$A_2=B_2$	$A_1<B_1$	X	X	X	X			
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0>B_0$	X	X	X			
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0<B_0$	X	X	X			
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	1	0	0			
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	0	1	0			
$A_3=B_3$	$A_2=B_2$	$A_1=B_1$	$A_0=B_0$	0	0	1			

8-Bit Comparator: -



Exercise:-

- **Write the truth table for 8-bit comparator and verify the same for the above circuit.**

Conclusion:-

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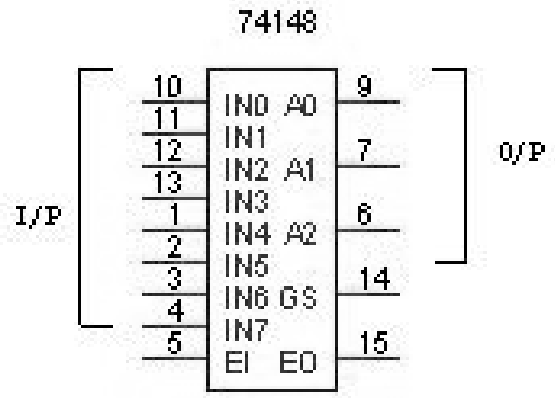
Signature of the staff in charge

PIN DETAILS:-



TRUTH TABLE:-

E_n	A	B	C	D	E	F	G	H	Q_2(V)	Q_1(V)	Q_0(V)	E_S(V)	E_O(V)
1	X	X	X	X	X	X	X	X	1	1	1	1	1
0	0	1	1	1	1	1	1	1	1	1	1	0	1
0	X	0	1	1	1	1	1	1	1	1	0	0	1
0	0	X	0	1	1	1	1	1	1	0	1	0	1
0	0	0	X	0	1	1	1	1	1	0	0	0	1
0	0	0	0	X	0	1	1	1	0	1	1	0	1
0	0	0	0	0	X	0	1	1	0	1	0	0	1
0	0	0	0	0	0	X	0	1	0	0	1	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	1	1	1	1	1	1	1	1	1	1	1	1	0

Experiment No: **DATE:___/__/____**

ENCODER & DECODER

AIM:-To convert a given octal input to th e binary output and to study the LED display using 7447 7-segment decoder/ driver.

APPARATUS REQUIRED: -

IC 74148, IC 7447, 7-segment displa y, etc.

PROCEDURE: - (Encoder)

1. **Connections are made as per circuit diagram.**
2. **The octal inputs are given at the corresponding pins.**
3. **The outputs are verified at the corresponding output pins.**

PROCEDURE: - (Decoder)

1. **Connections are made as per the circuit diagram.**
2. **Connect the pins of IC 7447 to the respec tive pins of the LED display board.**
3. **Give different combinations of the in puts and observe the decimal numbers displayed on the board.**

RESULT: -

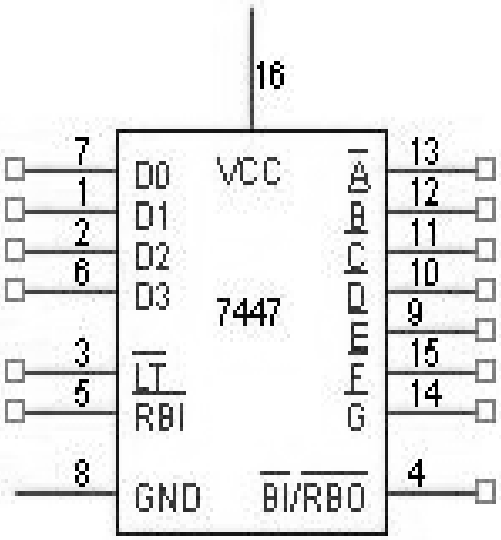
The given octal numbers are converted into binary numbers.

The given data is displayed using &-segment LED decode r.

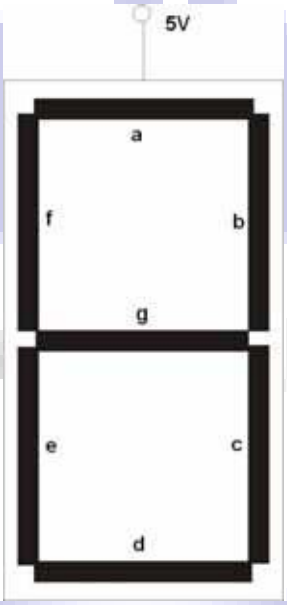
TABULAR COLUMN:-

Q4	Q3	Q2	Q1	O/P	Display	Glowing LEDs
0	0	0	0	0		a,b,c,d,e,f
0	0	0	1	1		b,c
0	0	1	0	2		a,b,d,e,g
0	0	1	1	3		a,b,c,d,g
0	1	0	0	4		b,c,f,g
0	1	0	1	5		a,c,d,f,g
0	1	1	0	6		a.c.d.e.f.g
0	1	1	1	7		a.b.c
1	0	0	0	8		a,b,c,d,e,f,g
1	0	0	1	9		a,b,c,d,f,g
1	0	1	0	10		d,e,g
1	0	1	1	11		c,d,g
1	1	0	0	12		c,d,e
1	1	0	1	13		a,g,d
1	1	1	0	14		d,e,f,g
1	1	1	1	15		blank

PIN DETAILS:-



DISPLAY:-



Conclusion:-

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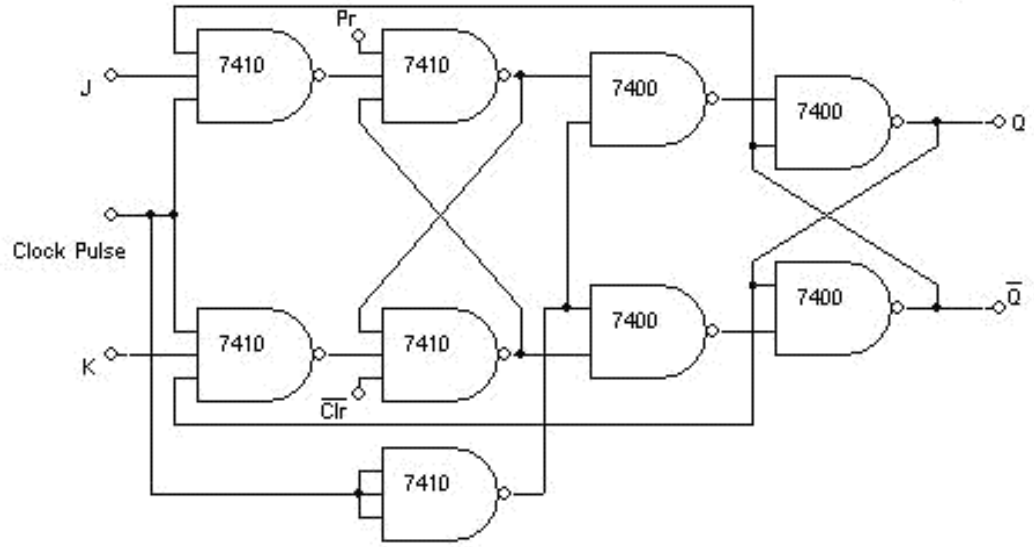
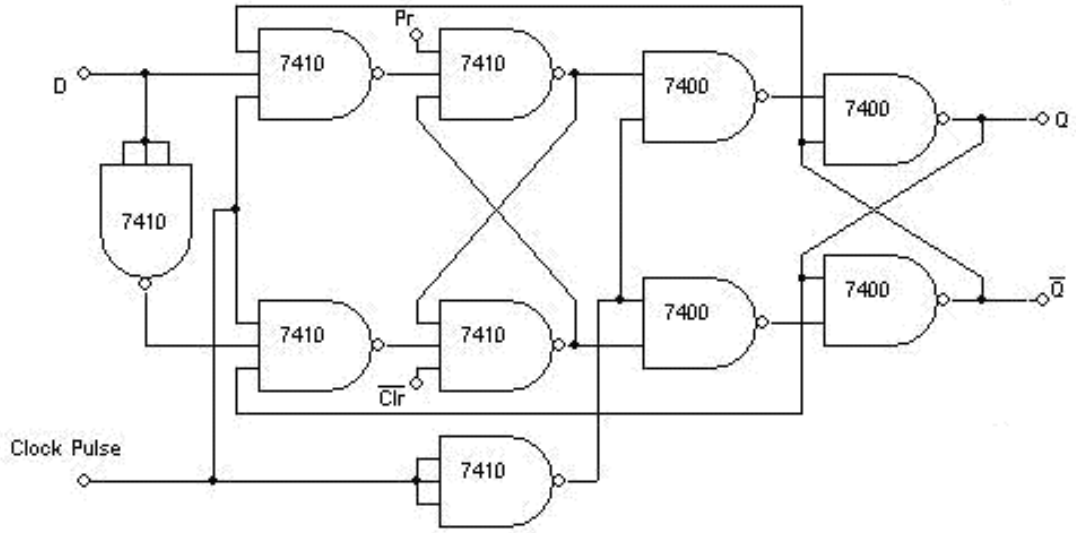
Signature of the staff in charge

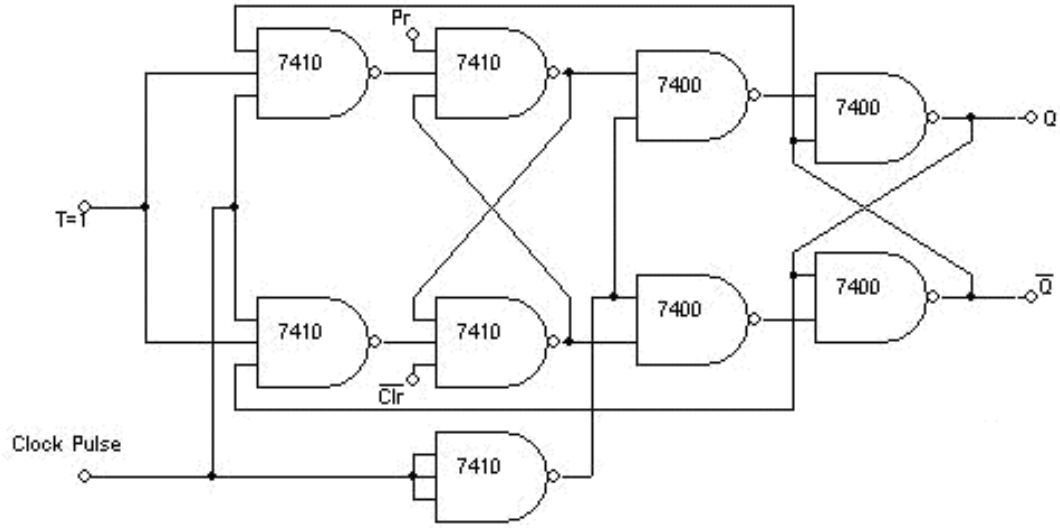
Circuit Diagram: - (Mas ter Slave JK Flip-Flop)



D Flip-Flop:-



T Flip-Flop:-



Experiment No: **Date:__/__/____**

FLIP-FLOP

Aim:- **Truth table verification of Flip-Flops :** **(i) JK Master Slave**
(ii) D- Type
(iii) T- Type.

Apparatus Required: -

IC 7410, IC 7400, etc.

Procedure: -

1. **Connections are made as per circuit diagram.**
2. **The truth table is verified for various combinations of inputs.**

Truth Table:- (Master Slave JK Flip-Flop)

Preset	Clear	J	K	Clock	Qn+1	$\overline{Qn+1}$	
0	1	X	X	X	1	0	Set
1	0	X	X	X	0	1	Reset
1	1	0	0	⎍	Qn	$\overline{Qn}$	No Change
1	1	0	1	⎍	0	1	Reset
1	1	1	0	⎍	1	0	Set
1	1	1	1	⎍	$\overline{Qn}$	Qn	Toggle

D Flip-Flop:-

Preset	Clear	D	Clock	Qn+1	$\overline{Qn+1}$
1	1	0	⎍	0	1
1	1	1	⎍	1	0

T Flip-Flop:-

Preset	Clear	T	Clock	Qn+1	$\overline{Qn+1}$
1	1	0	⎍	Qn	$\overline{Qn}$
1	1	1	⎍	$\overline{Qn}$	Qn

Exercise:-

- **Write the timing diagrams for all the above Flip-Flops**

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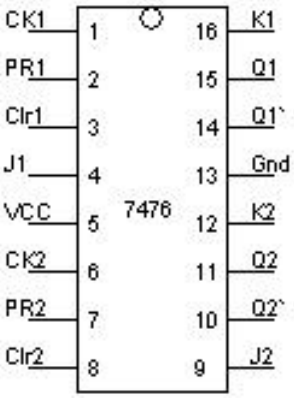
Signature of the staff in charge

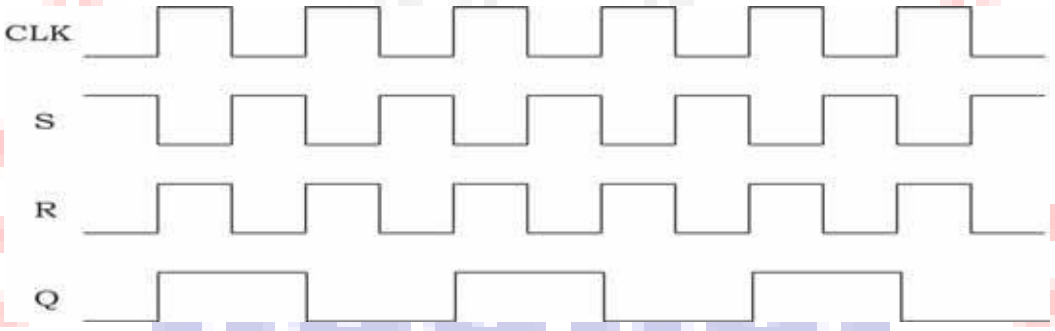
Pin Details: -



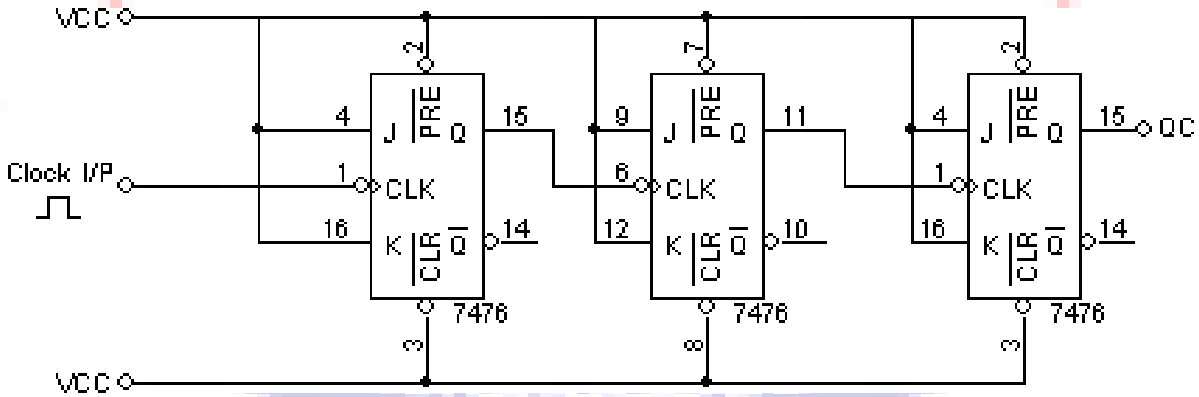
Truth Table:-

Clock	QC	QB	QA
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

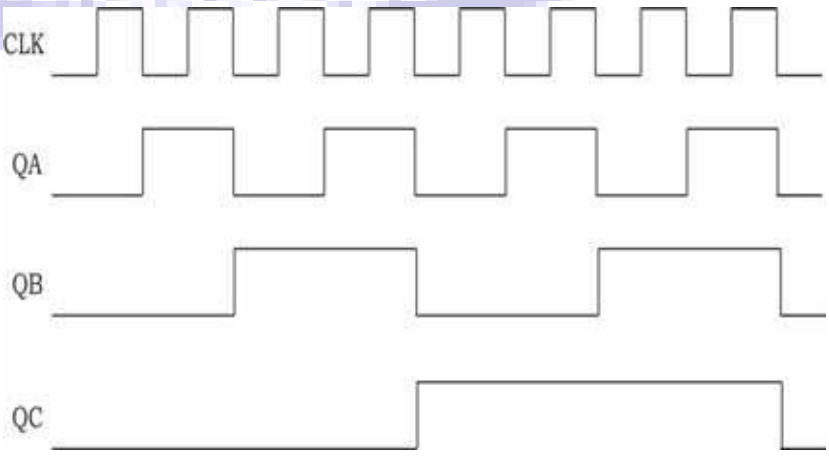
Timing Diagram:-



Circuit Diagram: - 3-Bit Asynchronous Up Counter



3-bit Asynchronous up counter			
Clock	QC	QB	QA
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0



9	0	0	1

Experiment No: **Date:__/__/____**

COUNTERS

Aim:- **Realization of 3-bit counters as a sequential circuit and Mod-N counter design (7476, 7490, 74192, 74193).**

Apparatus Required: -

IC 7408, IC 7476, IC 7490, IC 74192, IC 74193, IC 7400, IC 7416, IC 7432 etc.

Procedure: -

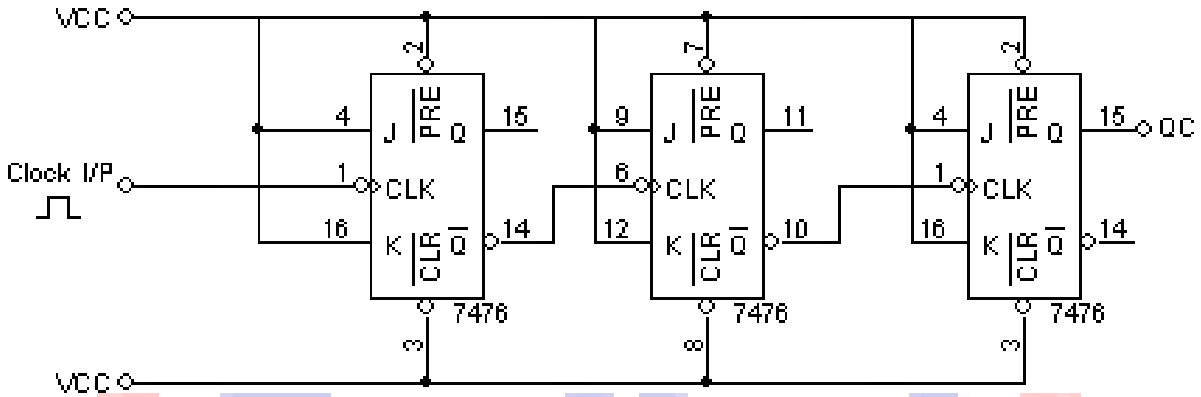
1. **Connections are made as per circuit diagram.**
2. **Clock pulses are applied one by one at the clock I/P and the O/P is observed at QA, QB & QC for IC 7476.**
3. **Truth table is verified.**

Procedure (IC 74192, IC 74193):-

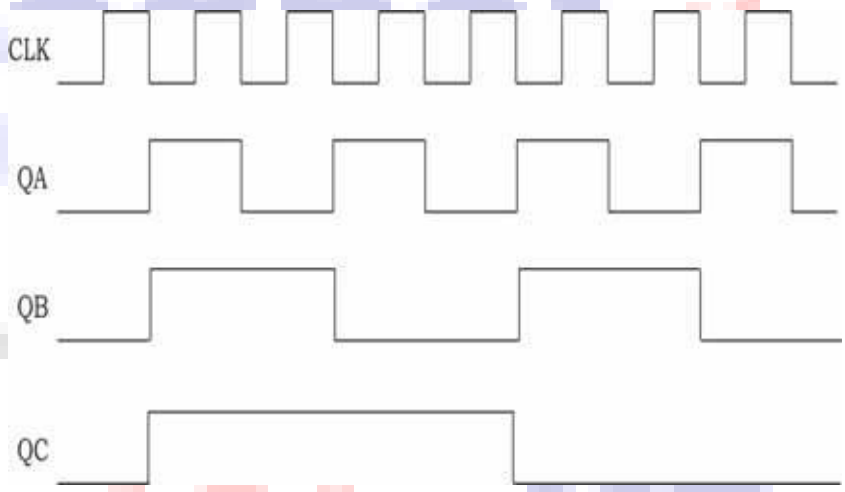
1. **Connections are made as per the circuit diagram except the connection from output of NAND gate to the load input.**
2. **The data (0011) = 3 is made available at the data i/ps A, B, C & D respectively.**
3. **The load pin made low so that the data 0011 appears at QD, QC, QB & QA respectively.**
4. **Now connect the output of the NAND gate to the load input.**
5. **Clock pulses are applied to "count up" pin and the truth table is verified.**
6. **Now apply (1100) = 12 for 12 to 5 counter and remaining is same as for 3 to 8 counter.**

7. **The pin diagram of IC 7419 2 is same as that of 74193. 74192 can be configured to count between 0 and 9 in either direction. The starting value can be any number between 0 and 9.**

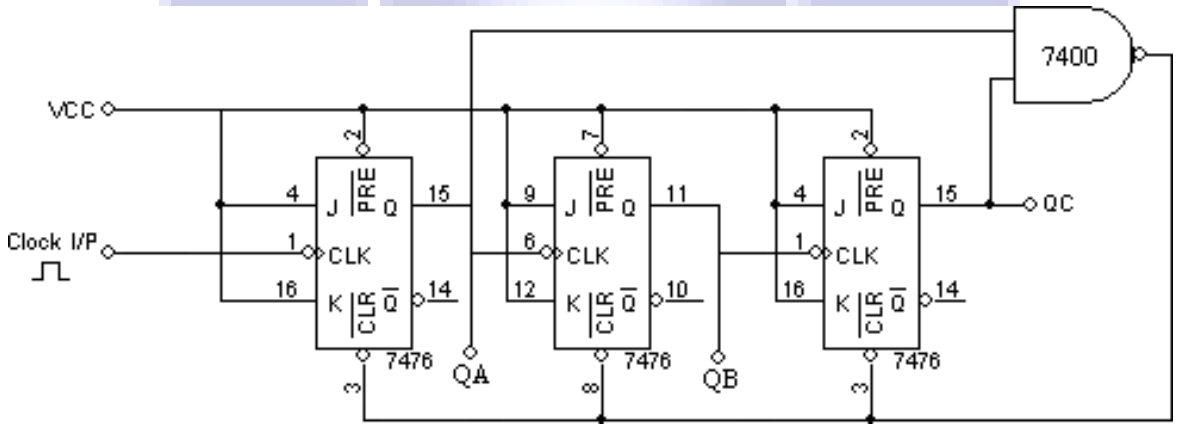
Circuit Diagram: - 3-Bit Asynchronous Down Counter



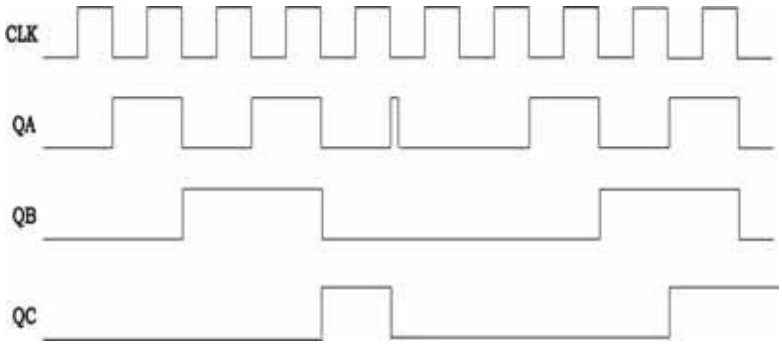
3-bit Asynchronous down counter			
Clock	**QC**	**QB**	**QA**
0	**1**	**1**	**1**
1	**1**	**1**	**0**
2	**1**	**0**	**1**
3	**1**	**0**	**0**
4	**0**	**1**	**1**
5	**0**	**1**	**0**
6	**0**	**0**	**1**
7	**0**	**0**	**0**
8	**1**	**1**	**1**
9	**1**	**1**	**0**



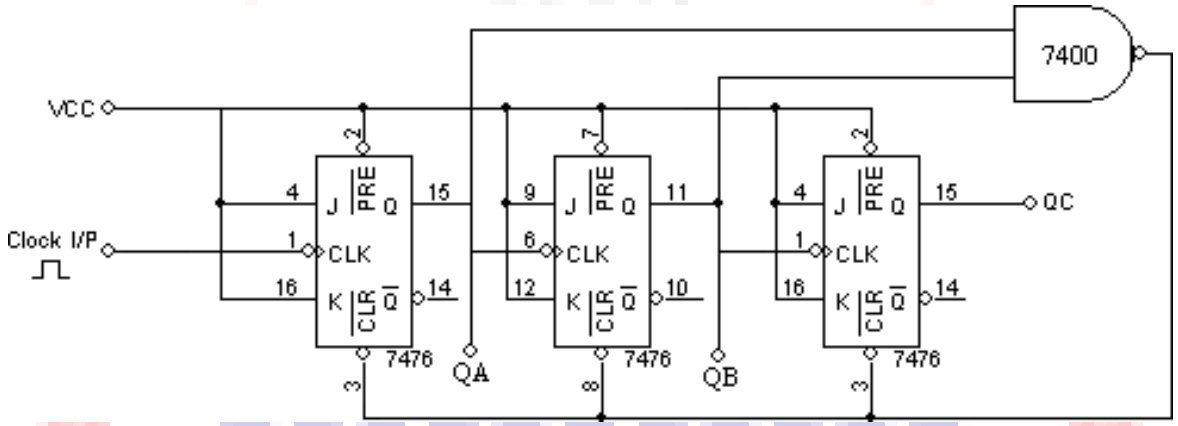
Mod 5 Asynchronous Counter:-



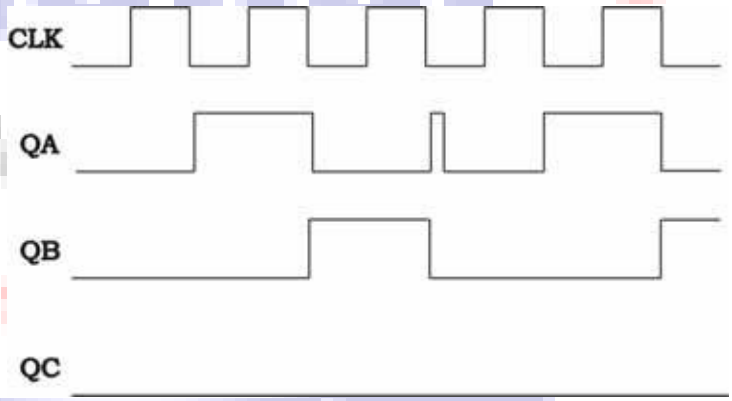
Mod 5 Asynchronous counter			
Clock	**QC**	**QB**	**QA**
0	**0**	**0**	**0**
1	**0**	**0**	**1**
2	**0**	**1**	**0**
3	**0**	**1**	**1**
4	**1**	**0**	**0**
5	**0**	**0**	**0**



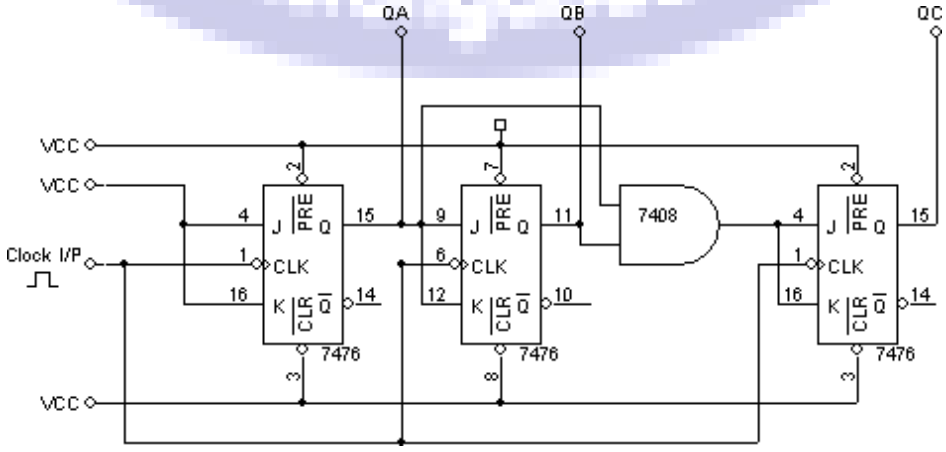
Mod 3 Asynchronous Counter:-

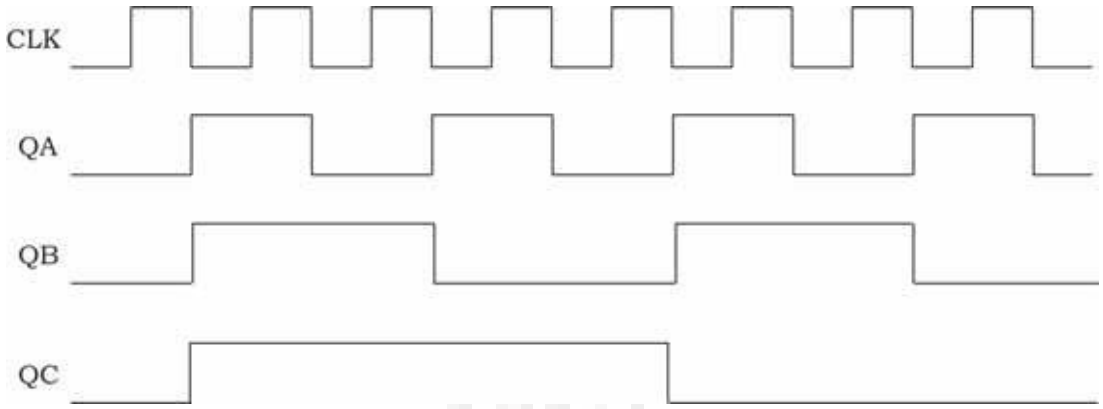


Mod 3 Asynchronous counter			
Clock	**QC**	**QB**	**QA**
0	**0**	**0**	**0**
1	**0**	**0**	**1**
2	**0**	**1**	**0**
3	**0**	**0**	**0**
4	**0**	**0**	**1**
5	**0**	**1**	**0**

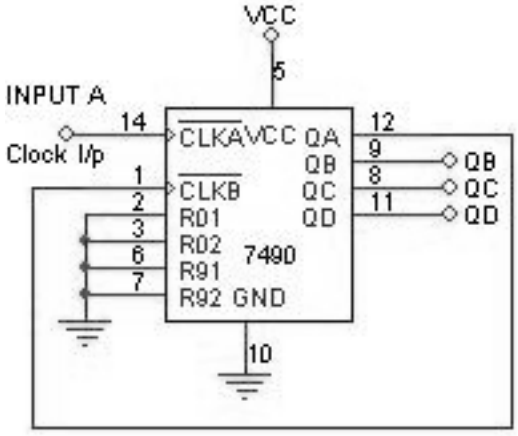


3-bit Synchronous Counter:-



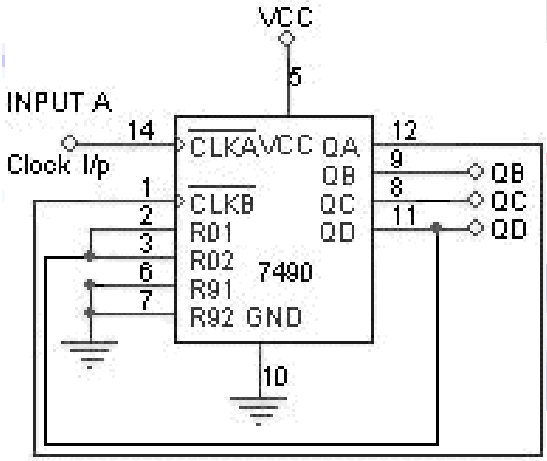


IC 7490 (Decade Counter):-



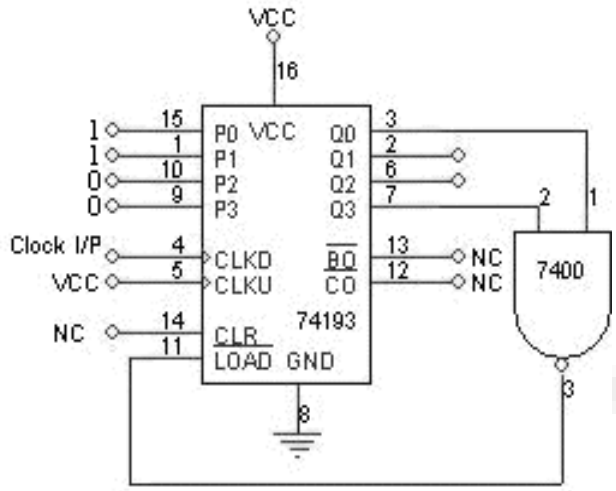
Clock	QD	QC	QB	QA
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	0	0	0	0

IC 7490 (MOD-8 Counter):-



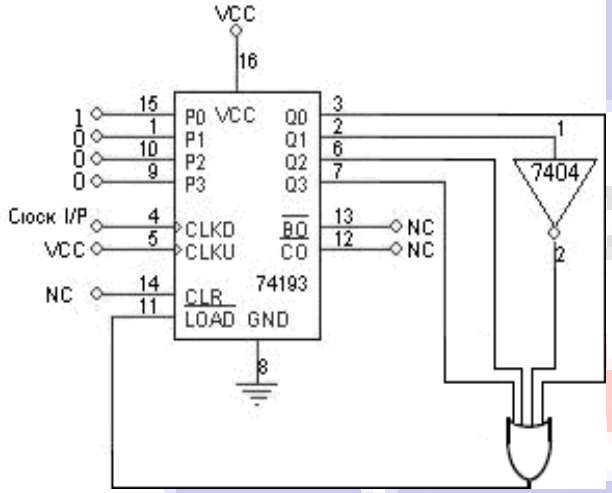
Clock	QD	QC	QB	QA
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	0	0	0	0
9	0	0	0	1

Circuit Diagram (IC 74193) To Count from 3 to 8:-



Clock	QD	QC	QB	QA	Count in Decimal
0	0	0	1	1	3
1	0	1	0	0	4
2	0	1	0	1	5
3	0	1	1	0	6
4	0	1	1	1	7
5	1	0	0	0	8
6	0	0	1	1	3
7	repeats				4

Circuit Diagram (IC 74193) To Count from 8 to 3:-

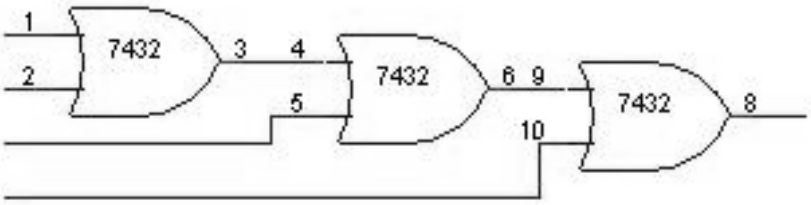


Clock	QD	QC	QB	QA	Count in Decimal
0	0	1	0	1	5
1	0	1	1	0	6
2	0	1	1	1	7
3	1	0	0	0	8
4	1	0	0	1	9
5	1	0	1	0	10
6	1	0	1	1	11
7	1	1	0	0	12
8	0	1	0	1	5
9	repeats				6

Function Table for 7490:-

Clock	R1	R2	S1	S2	QD	QC	QB	QA	
X	H	H	L	X	L	L	L	L	RESET
X	H	H	X	L	L	L	L	L	RESET
X	X	X	H	H	H	L	L	H	SET TO 9
⎍	X	L	X	L	COUNT				
⎍	L	X	L	X	COUNT				
⎍	L	X	X	L	COUNT				
⎍	X	L	L	X	COUNT				

4 I/P OR Gate can be realized as follows:-

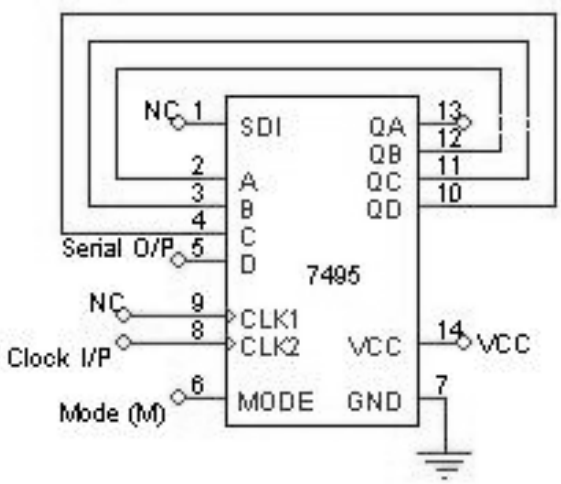


Conclusion:-

……

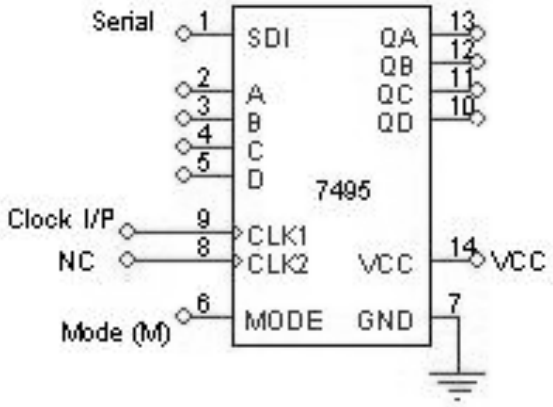
Signature of the staff in charge

Circuit Diagram: - Shift Left



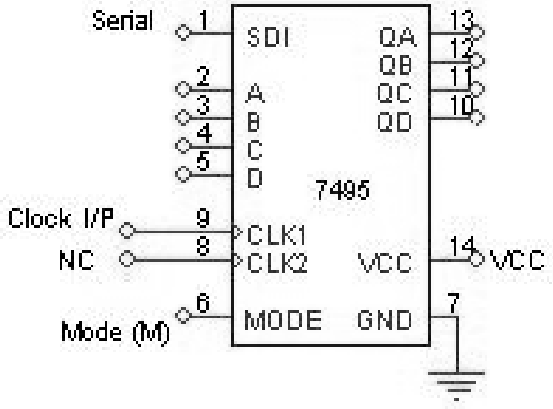
Clock	Serial i/p	QA	QB	QC	QD
1	1	X	X	X	1
2	0	X	X	1	0
3	1	X	1	0	1
4	1	1	0	1	1

SIPO (Right Shift):-



Clock	Serial i/p	QA	QB	QC	QD
1	0	0	X	X	X
2	1	1	0	X	X
3	1	1	1	0	X
4	1	1	1	1	0

SISO:-



Clock	Serial i/p	QA	QB	QC	QD
1	do=0	0	X	X	X
2	d1=1	1	0	X	X
3	d2=1	1	1	0	X
4	d3=1	1	1	1	0=do
5	X	X	1	1	1=d1
6	X	X	X	1	1=d2
7	X	X	X	X	1=d3

Experiment No: **Date:__/__/____**

SHIFT REGISTERS

Aim:- **Realization of 3-bit counters as a sequential circuit and Mod-N counter design (7476, 7490, 74192, 74193).**

Apparatus Required: -

IC 7495, etc.

Procedure: -

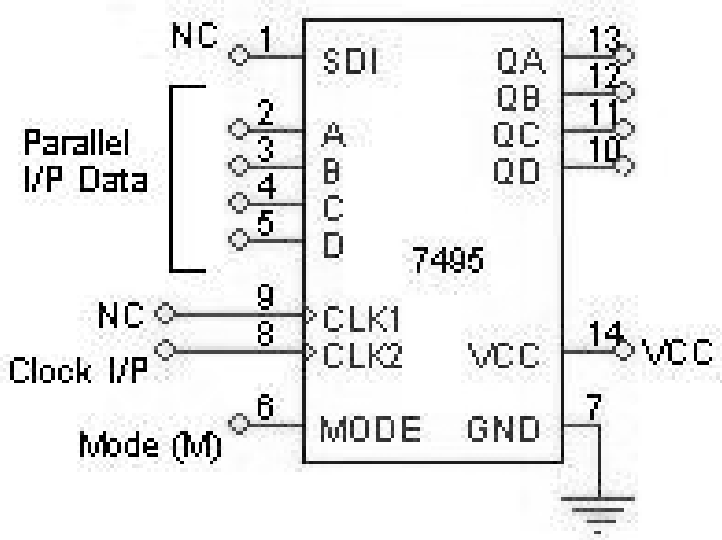
Serial In Parallel Out:-

1. **Connections are made as per circuit diagram.**
2. **Apply the data at serial i/p**
3. **Apply one clock pulse at clock 1 (Right Shift) observe this data at QA.**
4. **Apply the next data at serial i/p.**
5. **Apply one clock pulse at clock 2, observe that the data on QA will shift to QB and the new data applied will appear at QA.**
6. **Repeat steps 2 and 3 till all the 4 bits data are entered one by one into the shift register.**

Serial In Serial Out:-

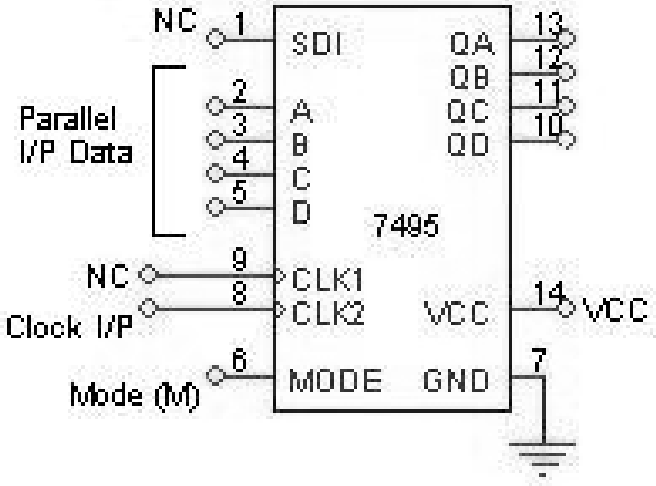
1. **Connections are made as per circuit diagram.**
2. **Load the shift register with 4 bits of data one by one serially.**
3. **At the end of 4th clock pulse the first data 'd0' appears at QD.**
4. **Apply another clock pulse; the second data 'd1' appears at QD.**
5. **Apply another clock pulse; the third data appears at QD.**
6. **Application of next clock pulse will enable the 4 th data 'd3' to appear at QD. Thus the data applied serially at the input comes out serially at QD**

PISO:-



Mode	Clock	Parallel i/p				Parallel o/p			
		A	B	C	D	QA	QB	QC	QD
1	1	1	0	1	1	1	0	1	1
0	2	X	X	X	X	X	1	0	1
0	3	X	X	X	X	X	X	1	0
0	4	X	X	X	X	X	X	X	1

PIPO:-



Clock	Parallel i/p				Parallel o/p			
	A	B	C	D	QA	QB	QC	QD
1	1	0	1	1	1	0	1	1

Parallel In Parallel Out:-

1. **Connections are made as per circuit diagram.**
2. **Apply the 4 bit data at A, B, C and D.**
3. **Apply one clock pulse at Clock 2 (Note: Mode control M=1).**
4. **The 4 bit data at A, B, C and D appears at QA, QB, QC and QD respectively.**

Parallel In Serial Out:-

1. **Connections are made as per circuit diagram.**
2. **Apply the desired 4 bit data at A, B, C and D.**
3. **Keeping the mode control M=1 apply one clock pulse. The data applied at A, B, C and D will appear at QA, QB, QC and QD respectively.**
4. **Now mode control M=0. Apply clock pulses one by one and observe the data coming out serially at QD.**

Left Shift:-

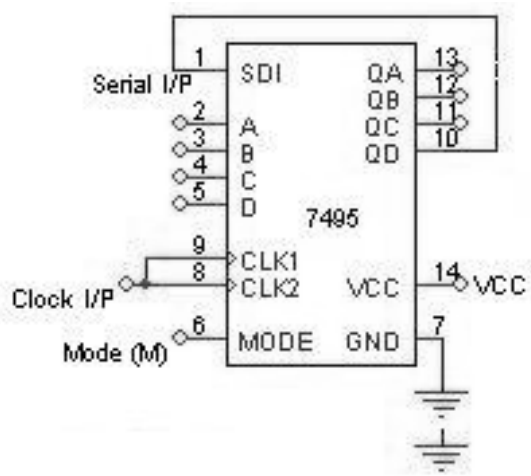
1. **Connections are made as per circuit diagram.**
2. **Apply the first data at D and apply on e clock pulse. This data appears at QD.**
3. **Now the second data is made availabl e at D and one clock pulse applied. The data appears at QD to QC an d the new data appears at QD.**
4. **Step 3 is repeated until all the 4 bits are entered one by one.**
5. **At the end 4th clock pulse the 4 bits are available at QA, QB, QC and QD.**

Conclusion:-

……..

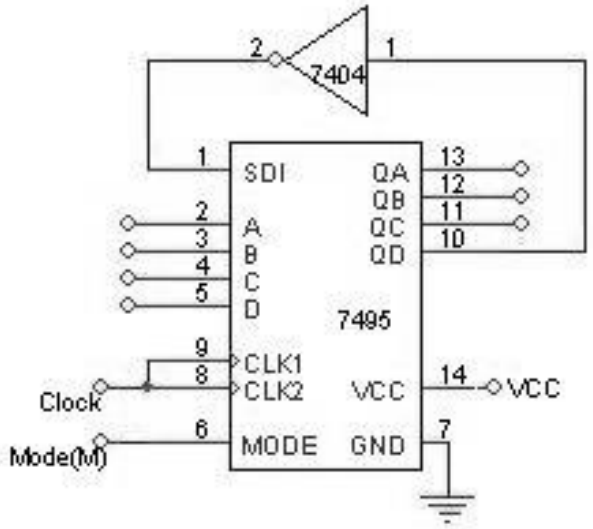
Signature of the staff in charge

Circuit Diagram: - Ring Counter



Mode	Clock	QA	QB	QC	QD
1	1	1	0	0	0
0	2	0	1	0	0
0	3	0	0	1	0
0	4	0	0	0	1
0	5	1	0	0	0
0	6	repeats			

Johnson Counter:-



Mode	Clock	QA	QB	QC	QD
1	1	1	0	0	0
0	2	1	1	0	0
0	3	1	1	1	0
0	4	1	1	1	1
0	5	0	1	1	1
0	6	0	0	1	1
0	7	0	0	0	1
0	8	0	0	0	0
0	9	1	0	0	0
0	10	repeats			

Experiment No: **Date:__/__/____**

JOHNSON COUNTERS / RING COUNTER

Aim:- **Design and testing of Ring counter/ Johnson counter.**

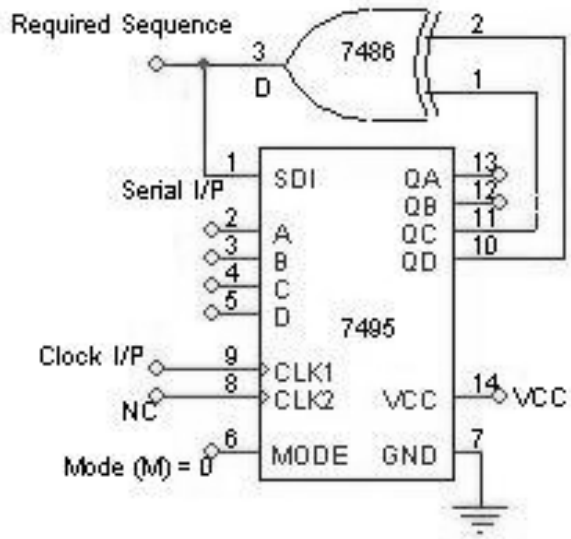
Apparatus Required: -

IC 7495, IC 7404, etc.

Procedure: -

1. **Connections are made as per the circuit diagram.**
2. **Apply the data 1000 at A, B, C and D respectively.**
3. **Keeping the mode M = 1, apply one clock pulse.**
4. **Now the mode M is made 0 and clock pulses are applied one by one and the truth table is verified.**
5. **Above procedure is repeated for Johnson counter also.**

Circuit Diagram: - Sequence Generator



Truth Table:-

Map Value	Clock	QA	QB	QC	QD	o/p D
15	1	1	1	1	1	0
7	2	0	1	1	1	0
3	3	0	0	1	1	0
1	4	0	0	0	1	1
8	5	1	0	0	0	0
4	6	0	1	0	0	0
2	7	0	0	1	0	1
9	8	1	0	0	1	1
12	9	1	1	0	0	0
6	10	0	1	1	0	1
11	11	1	0	1	1	0
5	12	0	1	0	1	1
10	13	1	0	1	0	1
13	14	1	1	0	1	1
14	15	1	1	1	0	1

Karnaugh Map for D:-

QCQD \ QA QB	00	01	11	10
00	0	0	0	0
01	1	1	1	1
11	0	0	0	0
10	1	1	1	1

Experiment No: **Date: __/_/____**

SEQUENCE GENERATOR

Aim:- **Design of Sequence Generator.**

Apparatus Required: -

IC 7495, IC 7486, etc.

Design:-

To generate a sequence of length S it is necessary to use at least N number of Flip-Flops, which satisfies the condition $S \leq 2^N - 1$.

The given sequence length S = 15.

Therefore N = 4.

Note: - There is no guarantee that the given sequence can be generated by 4 f/fs. If the sequence is not realizable by 4 f/fs then 5 f/fs must be used and so on.

Procedure: -

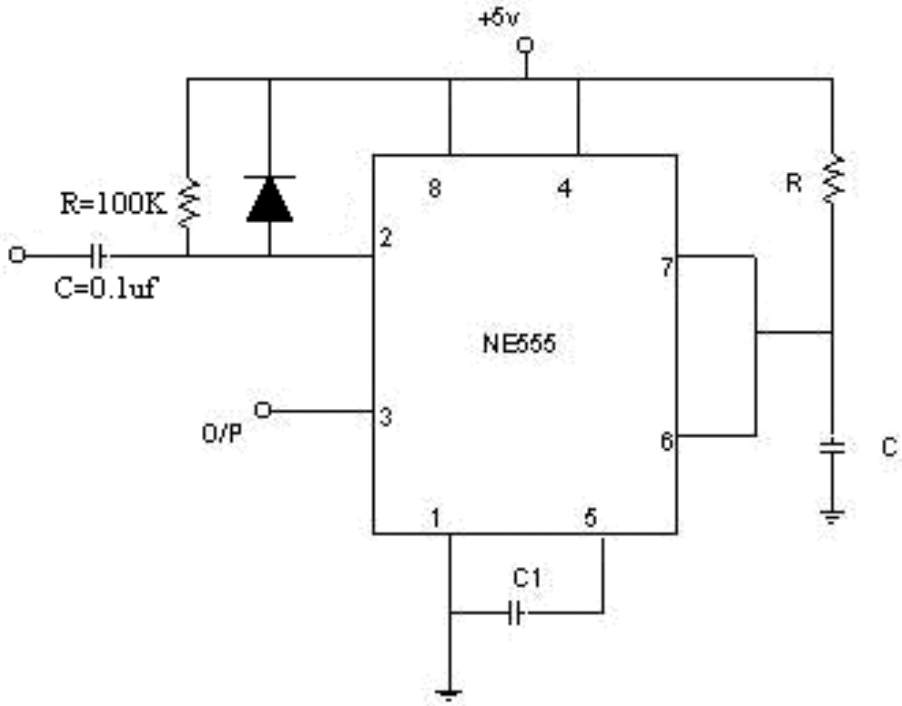
1. **Connections are made as per the circuit diagram.**
2. **Clock pulses are applied one by one and truth table is verified.**

Conclusion:-

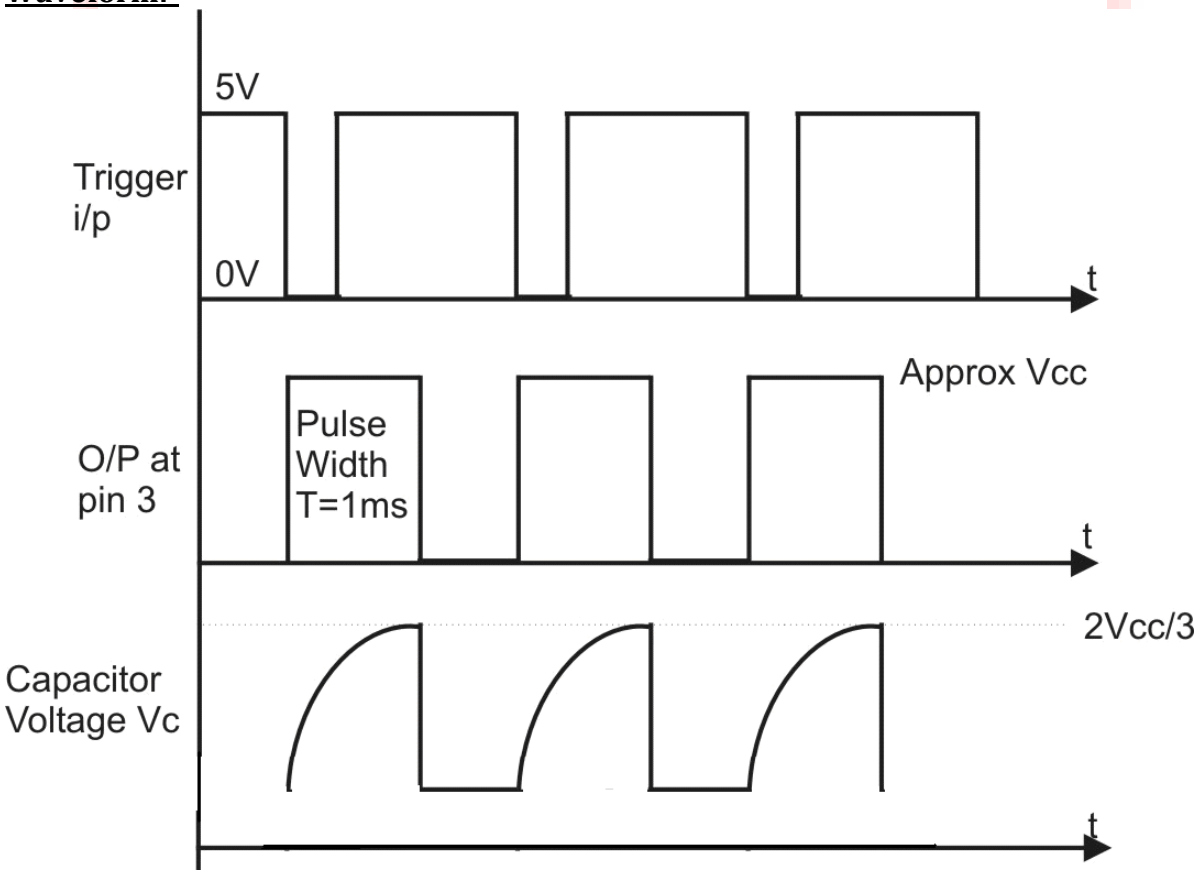
……

Signature of the staff in charge

Circuit Diagram: - Monostable Multivibrator



Waveform:-



Experiment No: **Date: __/_/____**

MULTIVIBRATORS

Aim:- **Design and testing of Monostable and Astable multivibrators using 555 timer.**

Apparatus Required: -

IC 555 timer, resistor, capacitor, etc.

Design:- (Monostable)

Given pulse width required = 1ms

Pulse width T = 1.1RC

Therefore 1ms = 1.1RC

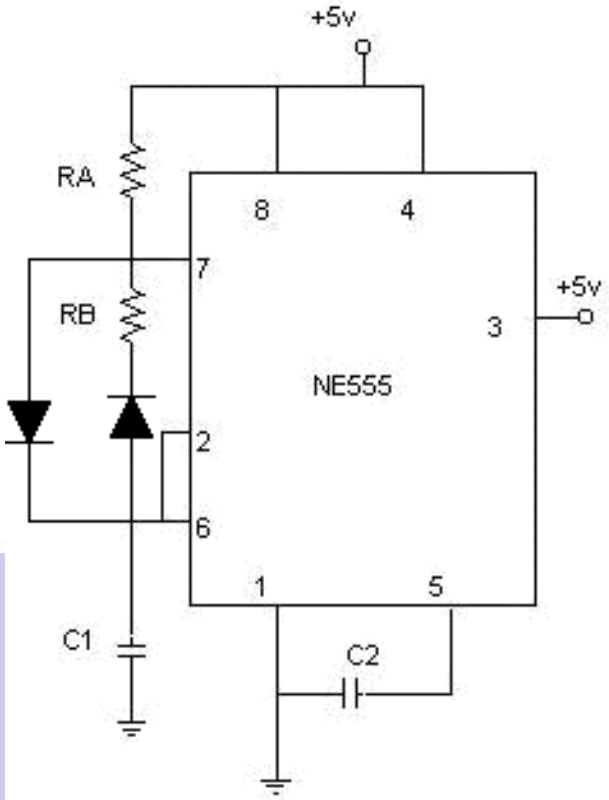
Let C = 0.1µf

Therefore $R = \frac{1\times10^{-3}}{1.1\times 0.1\times10^{-6}}$

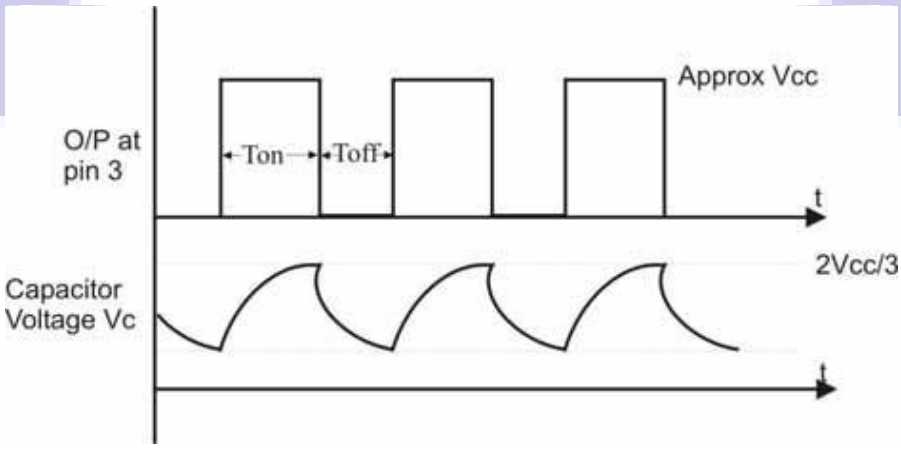
Procedure: -(Monostable)

1. **Connections are made as per the circuit diagram.**
2. **Triggering pulses are applied at pin 2.**
3. **The pulse width of the waveform at pin3 is measured and verified with the designed value.**

Astable Multivibrator:-



Wave form:-



Design:-

Ton = 0.69(R_A + R_B)C, Toff = 0.69 R_B C

Given; f = 10 KHz, duty cycle = 70%,

Therefore T = (1/f) = (1/10x10^3) = 0.1ms

D = (Ton/T) = 0.7

Ton = 0.7T = 0.7x0.1ms = 0.07ms

T = Ton + Toff

Therefore Toff = 0.03ms

Ton = 0.69 (R_A + R_B) C

Let C = 0.1µf

Therefore 0.07 x 10^{-3} = 0.69 (R_A + R_B) 0.1 x 10^{-6}

Therefore R_A + R_B = 1014 ohms

Toff = 0.69 R_B C

0.03 x 10^{-3} = 0.69 (R_B) 0.1 x 10^{-6}

Therefore R_B = 434.7 ohms

Therefore R_A = 579 ohms

Procedure: -

1. **Connections are made as per circuit diagram**
2. **Switch on the 5V power supply**
3. **Observe the waveforms at pin 3 on CRO, measure Ton, Toff, T and its amplitude.**
4. **Also observe capacitor voltage on CRO.**

Conclusion:-

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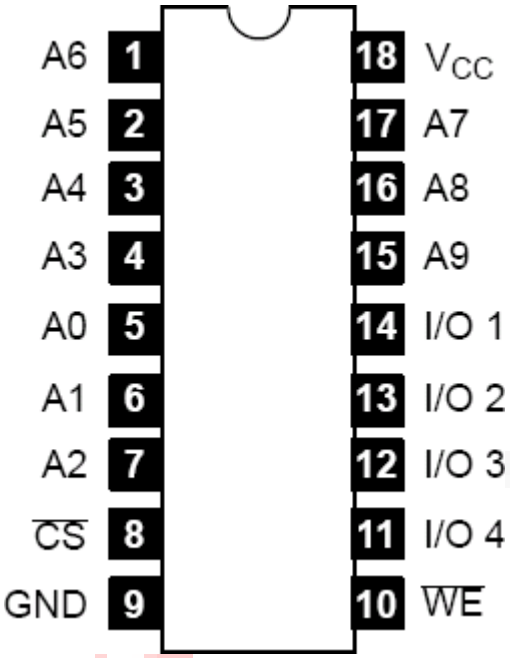
Signature of the staff in charge



Example for Data Input:-

Address Inputs			
A3	A2	A1	A0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1

Data Inputs			
I/O4	I/O3	I/O2	I/O1
0	0	1	0
0	1	0	0
0	1	0	1
0	1	1	0

Example for Data Output:-

Address Inputs			
A3	A2	A1	A0
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1

Data Outputs			
I/O4	I/O3	I/O2	I/O1
0	0	1	0
0	1	0	0
0	1	0	1
0	1	1	0

Experiment No: **Date:__/__/____**

STATIC RAM

Aim: - To conduct an experiment to store a set of data in a RAM using IC 2114 starting from location ------- to location-------- and retrieve the same data.

Apparatus Required: -

IC 2114, etc.

Procedure: -

1. **circuits connections are made to the appropriate pins of IC 2114**
2. **First you have to write the data and then read the data, for writing data make $\overline{WE}$ to low and $\overline{CS}$ input to low**
3. **for a 4-bit data select any address input from A0 to A9. for ex, select A3 to A0 and connect the data inputs / outputs i.e., I/O4 – I/O1**
4. **write a 4-bit data of your choice in each of the required address inputs or memory locations**
5. **by doing the above steps 2, 3 and 4 the data will be stored in the memory location**
6. **for reading data**
    a. **make $\overline{WE}$ to high and $\overline{CS}$ input to low**
    b. **disconnect the data inputs I/O4 – I/O1 from input lines and connect them to output lines to read the data**
    c. **and then give the address inputs of the data you have stored and observe the outputs through I/O4 – I/O1.**

Conclusion:-

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Signature of the staff in charge